

To all our customers

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Customer Support Dept.  
April 1, 2003

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# HN29V102414T-50H

1G AND type Flash Memory  
More than 32,113-sector (542,581,248-bit) × 2



ADE-203-1335A (Z)  
Rev. 1.0  
Apr. 5, 2002

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## Description

The Hitachi HN29V102414T-50H is a CMOS Flash Memory with AND type multi-level memory cells. It has fully automatic programming and erase capabilities with a single 3.0 V power supply. The functions are controlled by simple external commands. To fit the I/O card applications, the unit of programming and erase is as small as (2048 + 64) bytes. Initial available sectors of HN29V102414T-50H are more than 64,226 (98% of all sector address) and less than 65,536 sectors.

## Features

- On-board single power supply ( $V_{CC}$ ):  $V_{CC} = 2.7\text{ V to }3.6\text{ V}$
- Organization
  - AND Flash Memory: (2048 + 64) bytes × (More than 32,113 sectors) × 2
  - Data register: (2048 + 64) bytes × 2
- Multi-level memory cell
  - 2 bit/per memory cell
- Automatic programming
  - Sector program time: 1.0 ms (typ)
  - System bus free
  - Address, data latch function
  - Internal automatic program verify function
  - Status data polling function
- Automatic erase
  - Single sector erase time: 1.0 ms (typ)
  - System bus free
  - Internal automatic erase verify function
  - Status data polling function

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## HN29V102414T-50H

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- Erase mode
  - Single sector erase ((2048 + 64) byte unit)
- Fast serial read access time:
  - First access time: 50  $\mu$ s (max)
  - Serial access time: 50 ns (max)
- Low power dissipation:
  - $I_{CC1}$  = 2 mA (typ) (Read) (1-chip operation)  
 $I_{CC1}$  = 4 mA (typ) (Read) (2-chip operation)
  - $I_{CC2}$  = 20 mA (max) (Read) (1-chip operation)  
 $I_{CC2}$  = 40 mA (max) (Read) (2-chip operation)
  - $I_{SB2}$  = 50  $\mu$ A (max) (Standby) (1-chip operation)  
 $I_{SB2}$  = 100  $\mu$ A (max) (Standby) (2-chip operation)
  - $I_{CC3}/I_{CC4}$  = 40 mA (max) (Erase/Program) (1-chip operation)  
 $I_{CC3}/I_{CC4}$  = 80 mA (max) (Erase/Program) (2-chip operation)
  - $I_{SB3}$  = 20  $\mu$ A (max) (Deep standby) (1-chip operation)  
 $I_{SB3}$  = 40  $\mu$ A (max) (Deep standby) (2-chip operation)
- The following architecture is required for data reliability.
  - Error correction: more than 3-bit error correction per each sector read
  - Spare sectors: 1.8% (579 sectors)/chip (min) within usable sectors

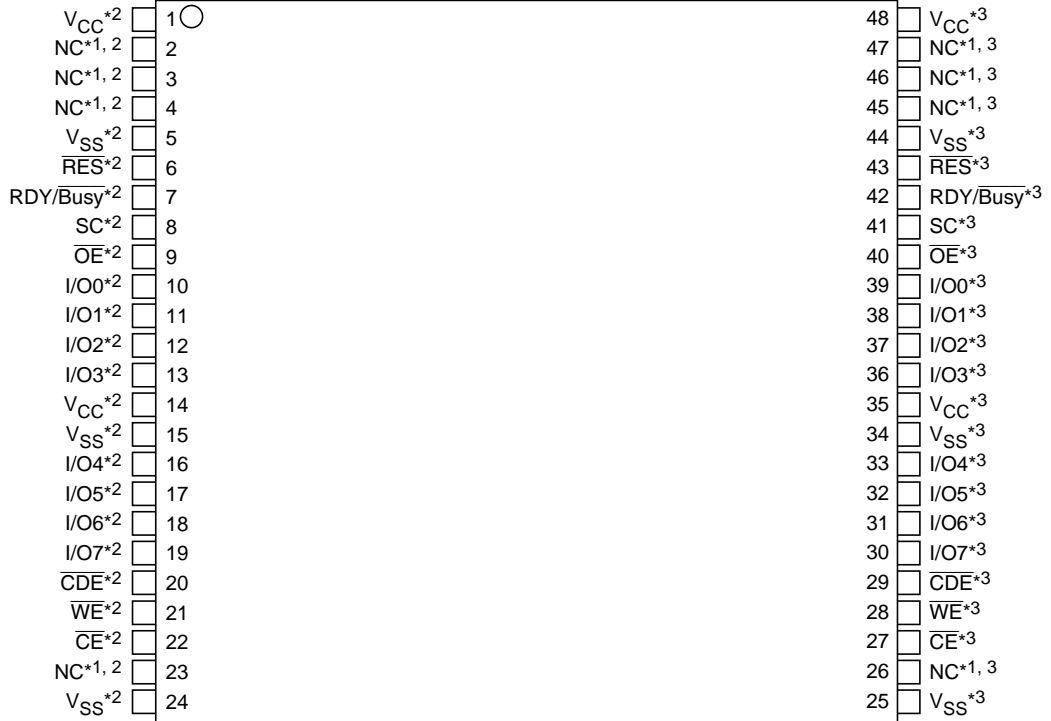
### Ordering Information

Type No.	Available sector	Package
HN29V102414T-50H	More than 64,226 sectors	12.0 $\times$ 20.00 mm <sup>2</sup> 0.5 mm pitch 48-pin plastic TSOP I (TFP-48DA)

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Pin Arrangement

48-pin TSOP



(Top view)

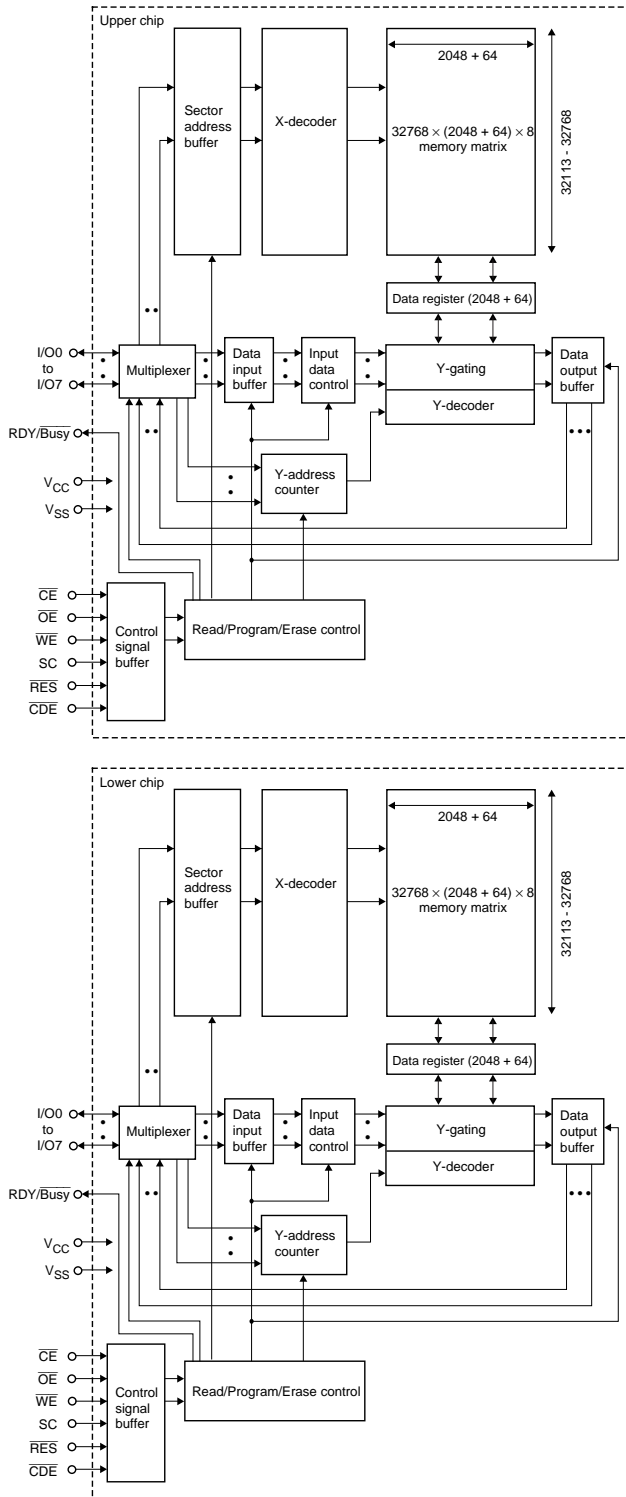
- Note: 1. This pin can be used as the  $V_{SS}$  pin.  
 2. Upper chip.  
 3. Lower chip.

**Pin Description**

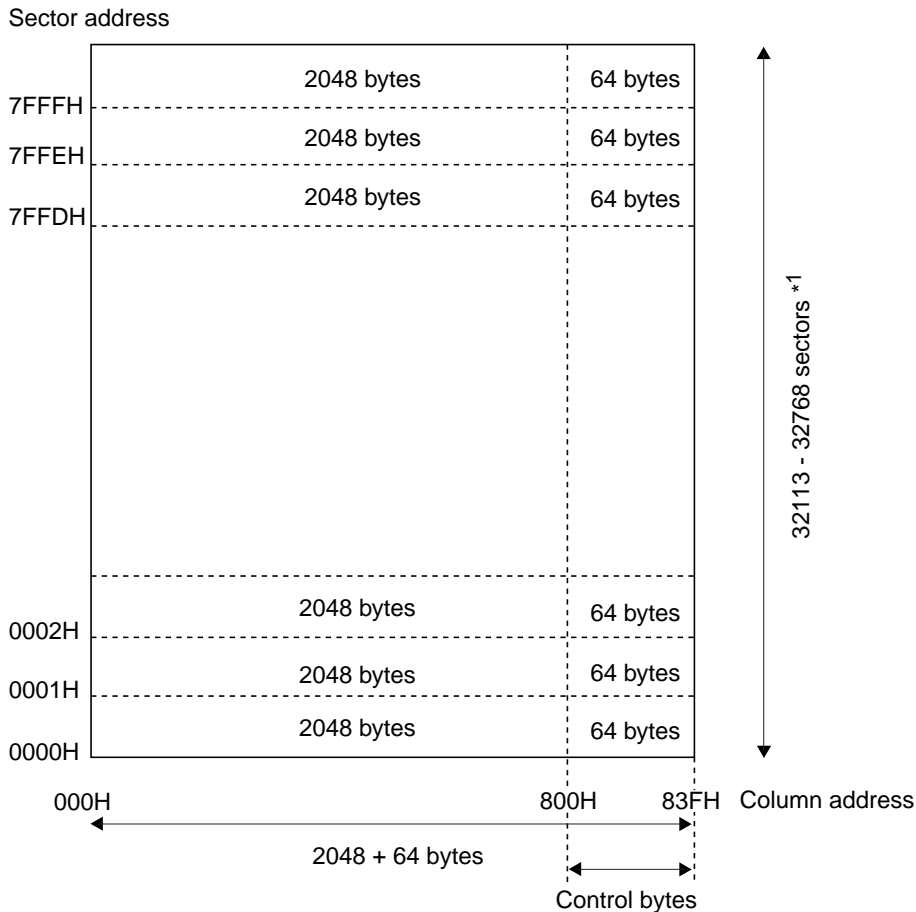
<b>Pin name</b>	<b>Function</b>
I/O0 to I/O7	Input/output
$\overline{\text{CE}}$	Chip enable
$\overline{\text{OE}}$	Output enable
$\overline{\text{WE}}$	Write enable
$\overline{\text{CDE}}$	Command data enable
$V_{\text{CC}}^{*1}$	Power supply
$V_{\text{SS}}^{*1}$	Ground
$\overline{\text{RDY/Busy}}$	Ready/ $\overline{\text{Busy}}$
$\overline{\text{RES}}$	Reset
SC	Serial clock
NC	No connection

Note: 1. All  $V_{\text{CC}}$  and  $V_{\text{SS}}$  pins should be connected to a common power supply and a ground, respectively.

Block Diagram



## Memory Map and Address



Address	Cycles	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
Sector address	SA (1): First cycle	A0	A1	A2	A3	A4	A5	A6	A7
	SA (2): Second cycle	A8	A9	A10	A11	A12	A13	A14	×*2
Column address	CA (1): First cycle	A0	A1	A2	A3	A4	A5	A6	A7
	CA (2): Second cycle	A8	A9	A10	A11	×	×	×	×

- Notes:
1. Some failed sectors may exist in the device. The failed sectors can be recognized by reading the sector valid data written in a part of the column address 800 to 83F (The specific address is TBD.). The sector valid data must be read and kept outside of the sector before the sector erase. When the sector is programmed, the sector valid data should be written back to the sector.
  2. An × means "Don't care". The pin level can be set to either  $V_{IL}$  or  $V_{IH}$ , referred to DC characteristics.



## Pin Function

**$\overline{CE}$ :**  $\overline{CE}$  is used to select the device. The status returns to the standby at the rising edge of  $\overline{CE}$  in the reading operation. However, the status does not return to the standby at the rising edge of  $\overline{CE}$  in the busy state in programming and erase operation.

**$\overline{OE}$ :** Memory data and status register data can be read, when  $\overline{OE}$  is  $V_{IL}$ .

**$\overline{WE}$ :** Commands and address are latched at the rising edge of  $\overline{WE}$ .

**SC:** Programming and reading data is latched at the rising edge of SC.

**$\overline{RES}$ :**  $\overline{RES}$  pin must be kept at the  $V_{ILR}$  ( $V_{SS} \pm 0.2$  V) level when  $V_{CC}$  is turned on and off. In this way, data in the memory is protected against unintentional erase and programming.  $\overline{RES}$  must be kept at the  $V_{IHR}$  ( $V_{CC} \pm 0.2$  V) level during any operations such as programming, erase and read.

**$\overline{CDE}$ :** Commands and data are latched when  $\overline{CDE}$  is  $V_{IL}$  and address is latched when  $\overline{CDE}$  is  $V_{IH}$ .

**RDY/ $\overline{Busy}$ :** The RDY/ $\overline{Busy}$  indicates the program/erase status of the flash memory. The RDY/ $\overline{Busy}$  signal is initially at a high impedance state. It turns to a  $V_{OL}$  level after the (40H) command in programming operation or the (B0H) command in erase operation. After the erase or programming operation finishes, the RDY/ $\overline{Busy}$  signal turns back to the high impedance state.

**I/O0 to I/O7:** The I/O pins are used to input data, address and command, and are used to output memory data and status register data.

## Mode Selection

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	SC	$\overline{RES}$	$\overline{CDE}$	RDY/ $\overline{Busy}$ *3	I/O0 to I/O7
Deep standby	$\times$ *4	$\times$	$\times$	$\times$	$V_{ILR}$	$\times$	$V_{OH}$	High-Z
Standby	$V_{IH}$	$\times$	$\times$	$\times$	$V_{IHR}$	$\times$	$V_{OH}$	High-Z
Output disable	$V_{IL}$	$V_{IH}$	$V_{IH}$	$\times$	$V_{IHR}$	$\times$	$V_{OH}$	High-Z
Status register read*1	$V_{IL}$	$V_{IL}$	$V_{IH}$	$\times$	$V_{IHR}$	$\times$	$V_{OH}$	Status register outputs
Command write*2	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IL}$	$V_{IHR}$	$V_{IL}$	$V_{OH}$	Din

- Notes: 1. Default mode after the power on is the status register read mode (refer to status transition). From I/O0 to I/O7 pins output the status, when  $\overline{CE} = V_{IL}$  and  $\overline{OE} = V_{IL}$  (conventional read operation condition).
2. Refer to the command definition. Data can be read, programmed and erased after commands are written in this mode.
3. The RDY/ $\overline{Busy}$  bus should be pulled up to  $V_{CC}$  to maintain the  $V_{OH}$  level while the RDY/ $\overline{Busy}$  pin outputs a high impedance.
4. An  $\times$  means "Don't care". The pin level can be set to either  $V_{IL}$  or  $V_{IH}$  referred to DC characteristics.

## Command Definition\*<sup>1, 2</sup>

Command		Bus cycles	First bus cycle		Second bus cycle		
			Operation mode* <sup>3</sup>	Data in	Operation mode	Data in	Data out
Read	Serial read (1) (Without CA)	3	Write	00H	Write	SA (1)* <sup>4</sup>	
		(With CA)	3 + 2h* <sup>6</sup>	Write			00H
	Serial read (2)	3	Write	F0H	Write	SA (1)* <sup>4</sup>	
	Read identifier codes	1	Write	90H	Read	ID* <sup>8, 9</sup>	
	Data recovery read	1	Write	01H	Read	Recovery data	
Auto erase	Single sector	4	Write	20H	Write	SA (1)* <sup>4</sup>	
Auto program	Program (1) (Without CA* <sup>7</sup> )	4	Write	10H	Write	SA (1)* <sup>4</sup>	
		(With CA* <sup>7</sup> )	4 + 2h* <sup>6</sup>	Write			10H
	Program (2)* <sup>10</sup>	4	Write	1FH	Write	SA (1)* <sup>4</sup>	
	Program (3) (Control bytes)* <sup>7</sup>	4	Write	0FH	Write	SA (1)* <sup>4</sup>	
	Program (4)	(Without CA* <sup>7</sup> )	4	Write	11H	Write	SA (1)* <sup>4</sup>
(With CA* <sup>7</sup> )		4 + 2h* <sup>6</sup>	Write	11H	SA (1)* <sup>4</sup>		
Reset		1	Write	FFH			
Clear status register		1	Write	50H			
Data recovery write		4	Write	12H	Write	SA (1)* <sup>4</sup>	

Command		Bus cycles	Third bus cycle		Fourth bus cycle	
			Operation mode	Data in	Operation mode	Data in
Read	Serial read (1) (Without CA)	3	Write	SA (2) <sup>*4</sup>		
		3 + 2h <sup>*6</sup>	Write	SA (2) <sup>*4</sup>	Write	CA (1) <sup>*5</sup>
	Serial read (2)	3	Write	SA (2) <sup>*4</sup>		
	Read identifier codes	1				
	Data recovery read	1				
Auto erase	Single sector	4	Write	SA (2) <sup>*4</sup>	Write	B0H <sup>*11</sup>
Auto program	Program (1) (Without CA <sup>*7</sup> )	4	Write	SA (2) <sup>*4</sup>	Write	40H <sup>*11, 12</sup>
		4 + 2h <sup>*6</sup>	Write	SA (2) <sup>*4</sup>	Write	CA (1)
	Program (2) <sup>*10</sup>	4	Write	SA (2) <sup>*4</sup>	Write	40H <sup>*11, 12</sup>
	Program (3) (Control bytes) <sup>*7</sup>	4	Write	SA (2) <sup>*4</sup>	Write	40H <sup>*11, 12</sup>
	Program (4) (Without CA <sup>*7</sup> )	4	Write	SA (2) <sup>*4</sup>	Write	40H <sup>*11, 12</sup>
4 + 2h <sup>*6</sup>		Write	SA (2) <sup>*4</sup>	Write	CA (1)	
Reset		1				
Clear status register		1				
Data recovery write		4	Write	SA (2) <sup>*4</sup>	Write	40H <sup>*11, 12</sup>

Command		Bus cycles	Fifth bus cycle		Sixth bus cycle		
			Operation mode	Data in	Operation mode	Data in	
Read	Serial read (1) (Without CA)	3					
		(With CA)	3 + 2h* <sup>6</sup>	Write	CA (2)* <sup>5</sup>		
	Serial read (2)	3					
	Read identifier codes	1					
	Data recovery read	1					
Auto erase	Single sector	4					
Auto program	Program (1) (Without CA* <sup>7</sup> )	4					
		(With CA* <sup>7</sup> )	4 + 2h* <sup>6</sup>	Write	CA (2)* <sup>5</sup>	Write	40H* <sup>11, 12</sup>
	Program (2)* <sup>10</sup>	4					
	Program (3) (Control bytes)* <sup>7</sup>	4					
	Program (4) (Without CA* <sup>7</sup> )	4					
		(With CA* <sup>7</sup> )	4 + 2h* <sup>6</sup>	Write	CA (2)	Write	40H* <sup>11, 12</sup>
Reset		1					
Clear status register		1					
Data recovery write		4					

- Notes:
1. Commands and sector address are latched at rising edge of  $\overline{WE}$  pulses. Program data is latched at rising edge of SC pulses.
  2. The chip is in the read status register mode when  $\overline{RES}$  is set to  $V_{IHR}$  first time after the power up.
  3. Refer to the command read and write mode in mode selection.
  4. SA (1) = Sector address (A0 to A7), SA (2) = Sector address (A8 to A14).
  5. CA (1) = Column address (A0 to A7), CA (2) = Column address (A8 to A11).  
( $0 \leq A11$  to  $A0 \leq 83FH$ )
  6. The variable h is the input number of times of set of CA (1) and CA (2) ( $1 \leq h \leq 2048 + 64$ ).  
Set of CA (1) and CA (2) can be input without limitation.
  7. By using program (1) and (3), data can additionally be programmed maximum 15 times for each sector before erase.
  8. ID = Identifier code; Manufacturer code (07H), Device code (9DH).
  9. The manufacturer identifier code is output when  $\overline{CDE}$  is low and the device identifier code is output when  $\overline{CDE}$  is high.
  10. Before program (2) operations, data in the programmed sector must be erased.
  11. No commands can be written during auto program and erase (when the  $RDY/\overline{Busy}$  pin outputs a  $V_{OL}$ ).
  12. The fourth or sixth cycle of the auto program comes after the program data input is complete.

## Mode Description

### Read

**Serial Read (1):** Memory data D0 to D2111 in the sector of address SA is sequentially read. Output data is not valid after the number of the SC pulse exceeds 2112. When CA is input, memory data D (m) to D (m + j) in the sector of address SA is sequentially read. Then output data is not valid after the number of the SC pulse exceeds (2112 to m). The mode turns back to the standby mode at any time when  $\overline{CE}$  is  $V_{IH}$ .

**Serial Read (2):** Memory data D2048 to D2111 in the sector of address SA is sequentially read. Output data is not valid after the number of the SC pulse exceeds 64. The mode turns back to the standby mode at any time when  $\overline{CE}$  is  $V_{IH}$ .

### Automatic Erase

**Single Sector Erase:** Memory data D0 to D2111 in the sector of address SA is erased automatically by internal control circuits. After the sector erase starts, the erasure completion can be checked through the  $RDY/\overline{Busy}$  signal and status data polling. All the bits in the sector are "1" after the erase. The sector valid data stored in a part of memory data D2048 to D2111 must be read and kept outside of the sector before the sector erase.

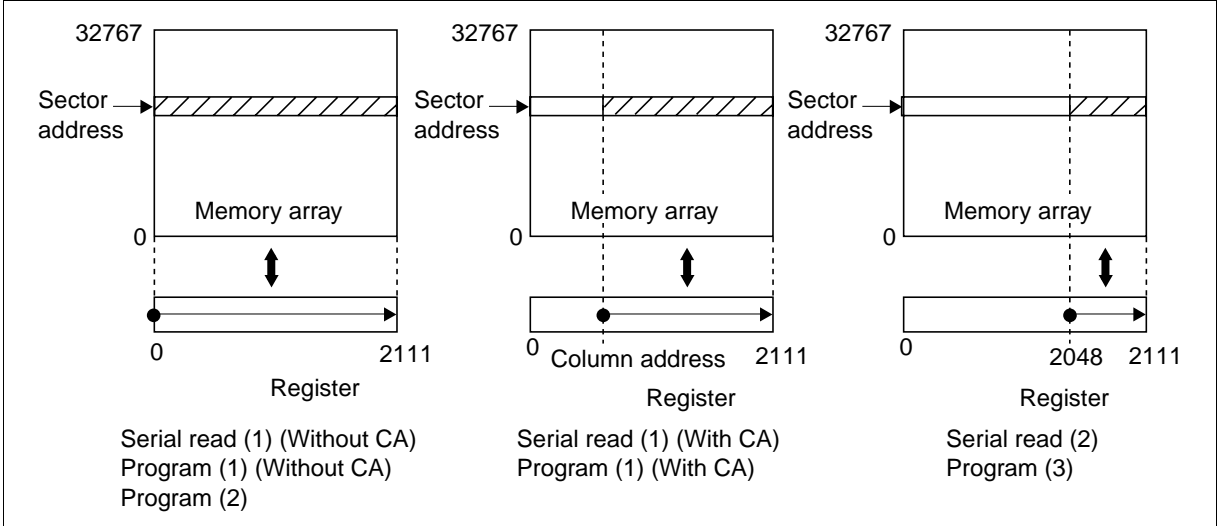
### Automatic Program

**Program (1):** Program data PD0 to PD2111 is programmed into the sector of address SA automatically by internal control circuits. When CA is input, program data PD (m) to PD (m + j) is programmed from CA into the sector of address SA automatically by internal control circuits. By using program (1), data can additionally be programmed 15 times for each sector before the following erase. When the column is programmed, the data of the column must be [FF]. After the programming starts, the program completion can be checked through the  $RDY/\overline{Busy}$  signal and status data polling. Programmed bits in the sector turn from "1" to "0" when they are programmed. The sector valid data should be included in the program data PD2048 to PD2111.

**Program (2):** Program data PD0 to PD2111 is programmed into the sector of address SA automatically by internal control circuits. After the programming starts, the program completion can be checked through the  $RDY/\overline{Busy}$  signal and status data polling. Programmed bits in the sector turn from "1" to "0" when they are programmed. The sector must be erased before programming. The sector valid data should be included in the program data PD2048 to PD2111.

**Program (3):** Program data PD2048 to PD2111 is programmed into the sector of address SA automatically by internal control circuits. By using program (3), data can additionally be programmed 15 times for each sector before the following erase. When the column is programmed, the data of the column must be [FF]. After the programming starts, the program completion can be checked through the  $RDY/\overline{Busy}$  signal and status data polling. Programmed bits in the sector turn from "1" to "0" when they are programmed.

**Program (4):** Program data PD0 to PD2111 is programmed into the sector of address SA automatically by internal control circuits. When CA is input, program data PD (m) to PD (m + j) is programmed from CA into the sector of address SA automatically by internal control circuits. By using program (4), data can be rewritten for each sector before the following erase. So the column data before programming operation are either "1" or "0". In this mode, E/W number of times must be counted whenever program (4) execute. After the programming starts, the program completion can be checked through the RDY/Busy signal and status data polling. The sector valid data should be included in the program data PD2048 to PD2111.



## Status Register Read

The status returns to the status register read mode from standby mode, when  $\overline{CE}$  and  $\overline{OE}$  is  $V_{IL}$ . In the status register read mode, I/O pins output the same operation status as in the status data polling defined in the function description.

## Identifier Read

The manufacturer and device identifier code can be read in the identifier read mode. The manufacturer and device identifier code is selected with  $\overline{CDE} V_{IL}$  and  $V_{IH}$ , respectively.

### **Data Recovery Read**

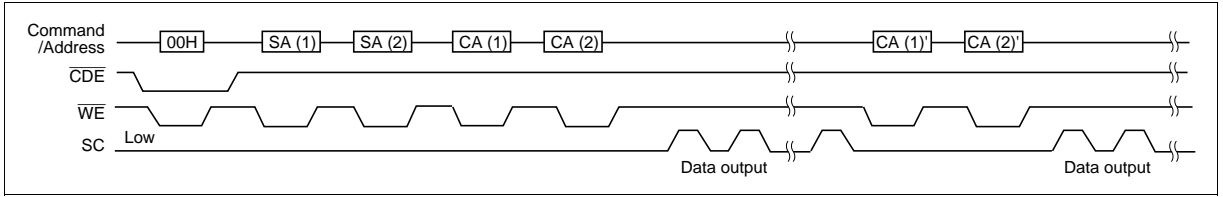
When the programming was an error, the program data can be read by using data recovery read. When an additional programming was an error, the data compounded of the program data and the origin data in the sector address SA can be read. Output data are not valid after the number of SA pulse exceeds 2112. The mode turns back to the standby mode at any time when  $\overline{CE}$  is  $V_{IH}$ . The read data are invalid when addresses are latched at a rising edge of  $\overline{WE}$  pulse after the data recovery read command is written.

### **Data Recovery Write**

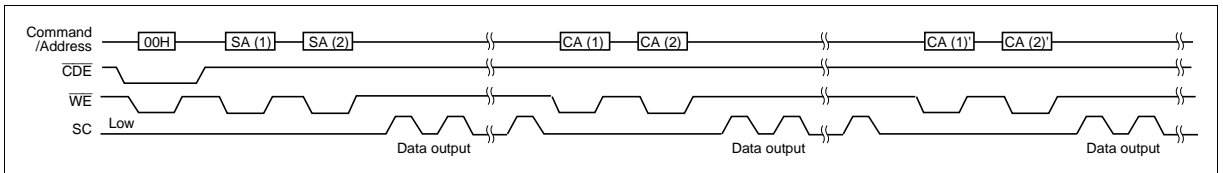
When the programming into a sector of address SA was an error, the program data can be rewritten automatically by internal control circuit into the other selected sector of address SA'. Since the data recovery write mode is internally Program (4) mode, rewritten sector of address SA' needs no sector erase before rewrite. After the data recovery write mode starts, the program completion can be checked through the RDY/ $\overline{Busy}$  signal and the status data polling.

## Command/Address/Data Input Sequence

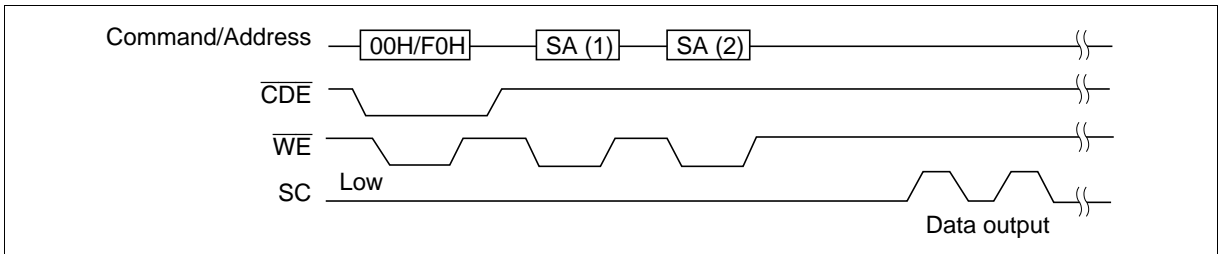
### Serial Read (1) (With CA before SC)



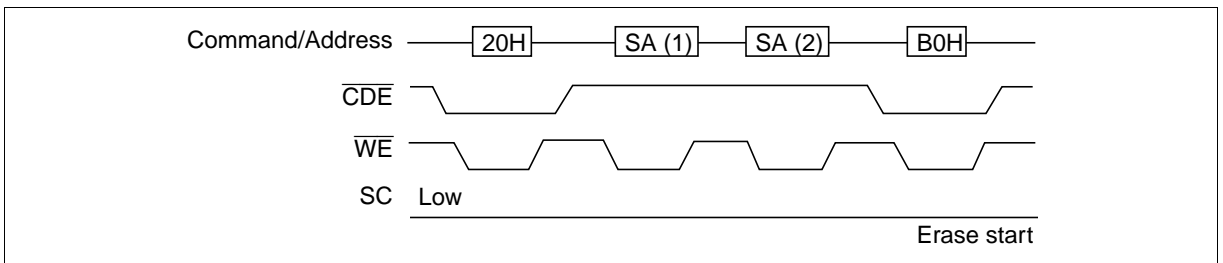
### Serial Read (1) (With CA after SC)



### Serial Read (1) (Without CA), (2)

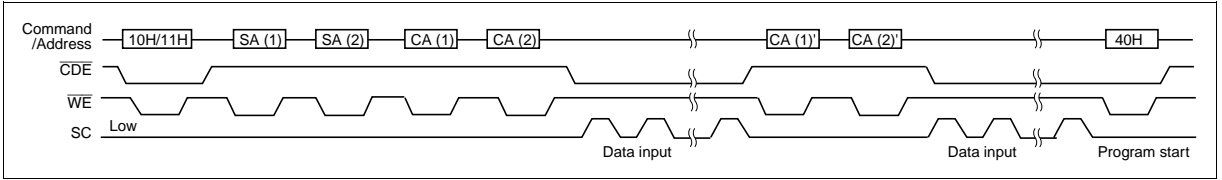


### Single Sector Erase

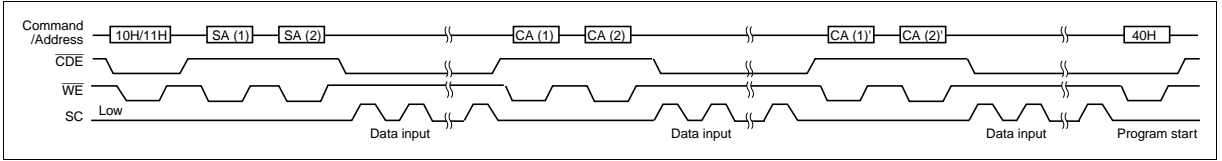




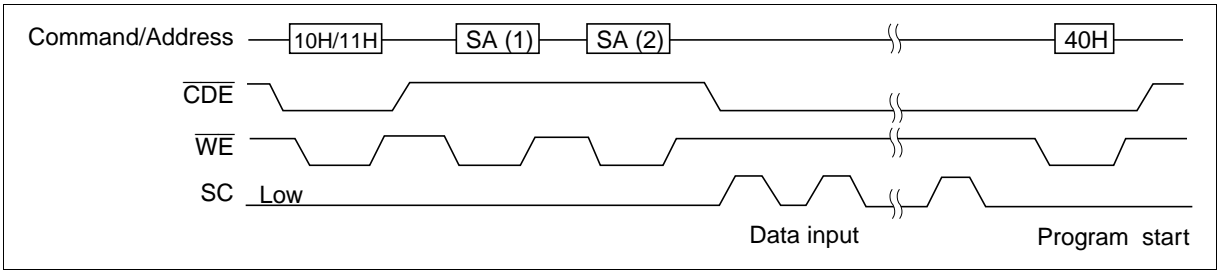
**Program (1), (4) (With CA before SC)**



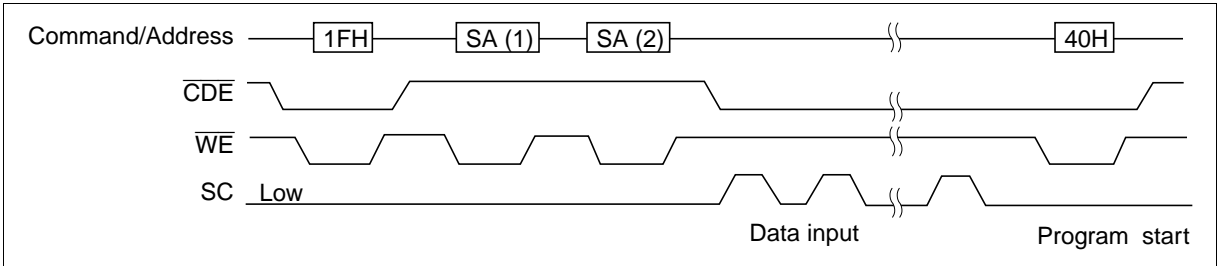
**Program (1), (4) (With CA after SC)**



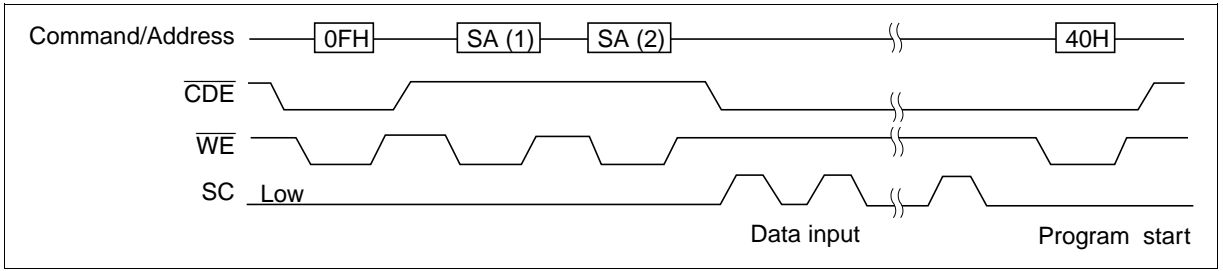
**Program (1), (4) (Without CA)**



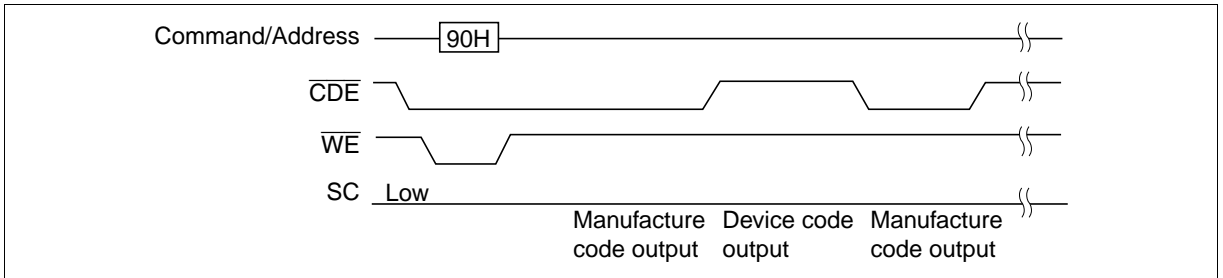
**Program (2)**



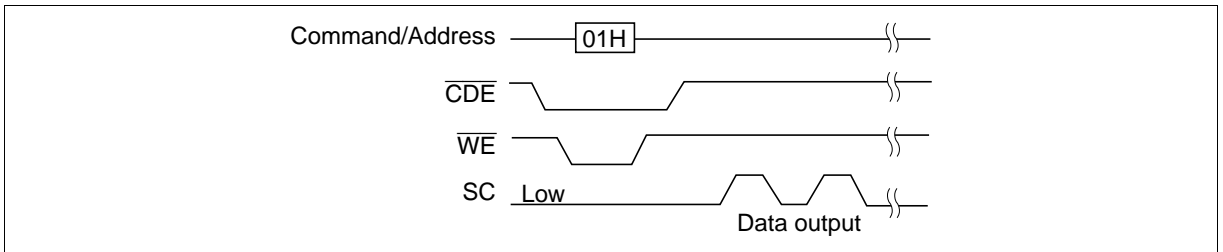
## Program (3)



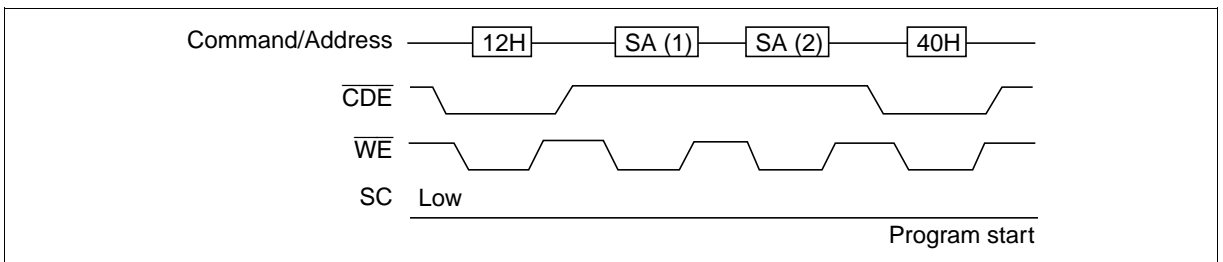
## ID Read Mode



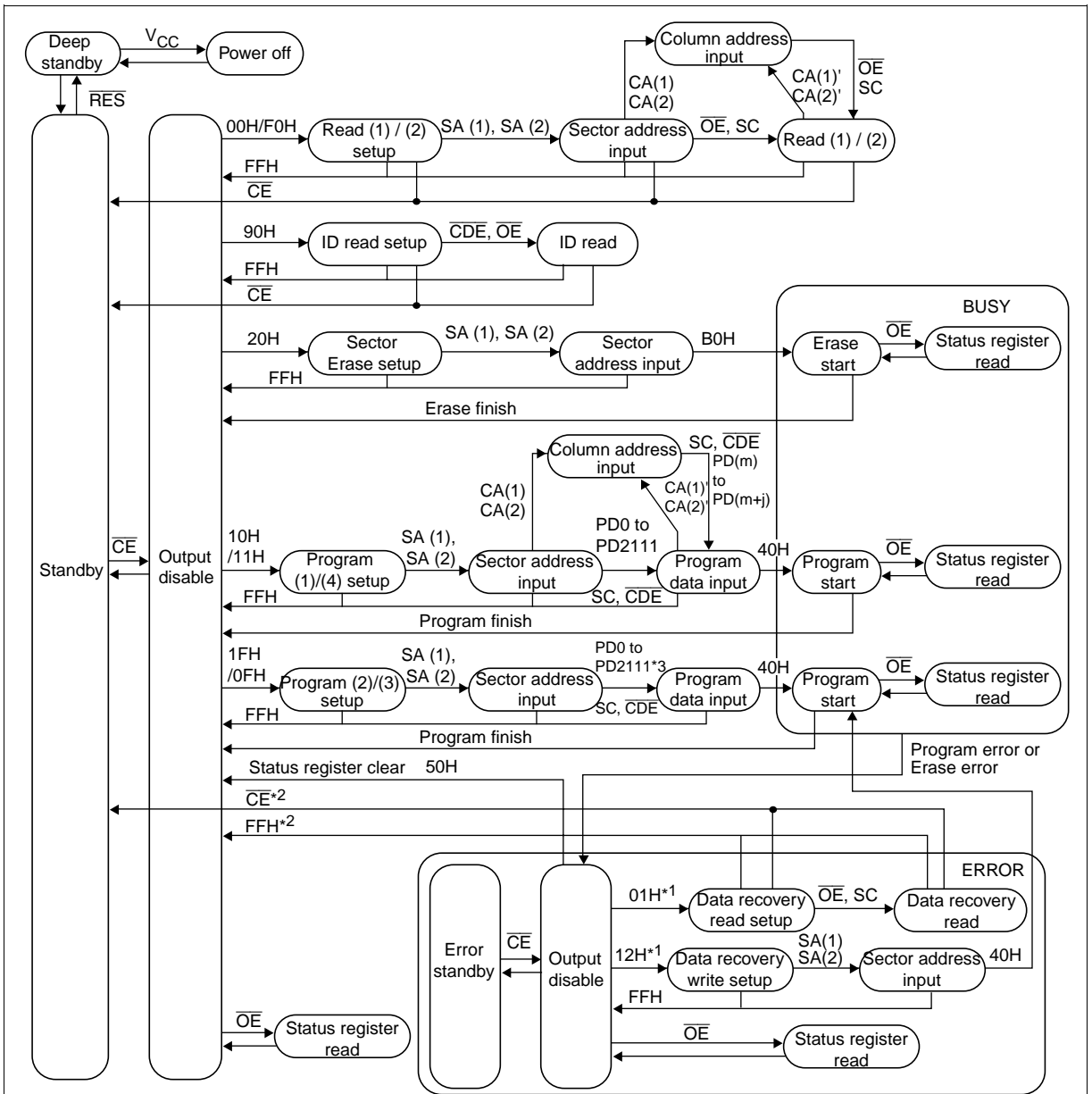
## Data Recovery Read Mode



## Data Recovery Write Mode



Status Transition



- Notes:
1. (01H)/(12H) Data recovery read/write can be used only for Program (1), (2), (3), (4) errors.
  2. When reset is done by  $\overline{CE}$  or FFH, error status flag is cleared.
  3. When Program (3) mode, input data is PD2048 to PD2111.

**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit	Notes
V <sub>CC</sub> voltage	V <sub>CC</sub>	-0.6 to +4.6	V	1
V <sub>SS</sub> voltage	V <sub>SS</sub>	0	V	
All input and output voltages	V <sub>in</sub> , V <sub>out</sub>	-0.6 to +4.6	V	1, 2
Operating temperature range	T <sub>opr</sub>	0 to +70	°C	
Storage temperature range	T <sub>stg</sub>	-65 to +125	°C	3
Storage temperature under bias	T <sub>bias</sub>	-10 to +80	°C	

Notes: 1. Relative to V<sub>SS</sub>.

2. V<sub>in</sub>, V<sub>out</sub> = -2.0 V for pulse width ≤ 20 ns.

3. Device storage temperature range before programming.

**Capacitance (T<sub>a</sub> = 25°C, f = 1 MHz)**

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	C <sub>in</sub>	—	—	6	pF	V <sub>in</sub> = 0 V
Output capacitance	C <sub>out</sub>	—	—	12	pF	V <sub>out</sub> = 0 V

**DC Characteristics** ( $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ ,  $T_a = 0 \text{ to } +70^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	$I_{LI}$	—	—	2	$\mu\text{A}$	$V_{in} = V_{SS} \text{ to } V_{CC}$
Output leakage current	$I_{LO}$	—	—	2	$\mu\text{A}$	$V_{out} = V_{SS} \text{ to } V_{CC}$
Standby $V_{CC}$ current (1-chip operation)	$I_{SB1}$	—	0.3	1	mA	$\overline{CE} = V_{IH}$
(2-chip operation)	$I_{SB1}$	—	0.6	2	mA	
(1-chip operation)	$I_{SB2}$	—	30	50	$\mu\text{A}$	$\overline{CE} = V_{CC} \pm 0.2 \text{ V}$ , $\overline{RES} = V_{CC} \pm 0.2 \text{ V}$
(2-chip operation)	$I_{SB2}$	—	60	100	$\mu\text{A}$	
Deep standby $V_{CC}$ current (1-chip operation)	$I_{SB3}$	—	1	20	$\mu\text{A}$	$\overline{RES} = V_{SS} \pm 0.2 \text{ V}$
(2-chip operation)	$I_{SB3}$	—	2	40	$\mu\text{A}$	
Operating $V_{CC}$ current (1-chip operation)	$I_{CC1}$	—	2	20	mA	$I_{out} = 0 \text{ mA}$ , $f = 0.2 \text{ MHz}$
(2-chip operation)	$I_{CC1}$	—	4	40	mA	
(1-chip operation)	$I_{CC2}$	—	10	20	mA	$I_{out} = 0 \text{ mA}$ , $f = 20 \text{ MHz}$
(2-chip operation)	$I_{CC2}$	—	20	40	mA	
Operating $V_{CC}$ current (Program) (1-chip operation)	$I_{CC3}$	—	20	40	mA	In programming
(2-chip operation)	$I_{CC3}$	—	40	80	mA	
Operating $V_{CC}$ current (Erase) (1-chip operation)	$I_{CC4}$	—	20	40	mA	In erase
(2-chip operation)	$I_{CC4}$	—	40	80	mA	
Input voltage	$V_{IL}$	$-0.3^{*1,2}$	—	0.8	V	
	$V_{IH}$	2.0	—	$V_{CC} + 0.3^{*3}$	V	
Input voltage ( $\overline{RES}$ pin)	$V_{ILR}$	-0.2	—	0.2	V	
	$V_{IHR}$	$V_{CC} - 0.2$	—	$V_{CC} + 0.2$	V	
Output voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 2 \text{ mA}$
	$V_{OH}$	2.4	—	—	V	$I_{OH} = -2 \text{ mA}$

Notes: 1.  $V_{IL}$  min = -1.0 V for pulse width  $\leq 50 \text{ ns}$  in the read operation.  $V_{IL}$  min = -2.0 V for pulse width  $\leq 20 \text{ ns}$  in the read operation.

2.  $V_{IL}$  min = -0.6 V for pulse width  $\leq 20 \text{ ns}$  in the erase/data programming operation.

3.  $V_{IH}$  max =  $V_{CC} + 1.5 \text{ V}$  for pulse width  $\leq 20 \text{ ns}$ . If  $V_{IH}$  is over the specified maximum value, the operations are not guaranteed.

## AC Characteristics ( $V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$ , $T_a = 0$ to $+70^\circ\text{C}$ )

### Test Conditions

- Input pulse levels:  $0.4\text{ V}/2.4\text{ V}$
- Input pulse levels for  $\overline{\text{RES}}$ :  $0.2\text{ V}/V_{CC} - 0.2\text{ V}$
- Input rise and fall time:  $\leq 5\text{ ns}$
- Output load: 1 TTL gate + 100 pF (Including scope and jig.)
- Reference levels for measuring timing: 0.8 V, 1.8 V

**Power on and off, Serial Read Mode**

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Notes
Write cycle time	$t_{CWC}$	120	—	—	ns		
Serial clock cycle time	$t_{SCC}$	50	—	—	ns		
$\overline{CE}$ setup time	$t_{CES}$	0	—	—	ns		
$\overline{CE}$ hold time	$t_{CEH}$	0	—	—	ns		
Write pulse time	$t_{WP}$	60	—	—	ns	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$	
Write pulse high time	$t_{WPH}$	40	—	—	ns		
Address setup time	$t_{AS}$	50	—	—	ns		
Address hold time	$t_{AH}$	10	—	—	ns		
Data setup time	$t_{DS}$	50	—	—	ns		
Data hold time	$t_{DH}$	10	—	—	ns		
SC to output delay	$t_{SAC}$	—	—	50	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$	
$\overline{OE}$ setup time for SC	$t_{OES}$	0	—	—	ns		
$\overline{OE}$ low to output low-Z	$t_{OEL}$	0	—	40	ns		
$\overline{OE}$ setup time before read	$t_{OER}$	100	—	—	ns		
$\overline{OE}$ setup time before command write	$t_{OEWS}$	0	—	—	ns		
SC to output hold	$t_{SH}$	15	—	—	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$	
$\overline{OE}$ high to output float	$t_{DF}$	—	—	40	ns	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$	1
$\overline{WE}$ to SC delay time	$t_{WSD}$	50	—	—	$\mu$ s		2
$\overline{RES}$ to $\overline{CE}$ setup time	$t_{RP}$	0.3	—	—	ms		
SC to $\overline{OE}$ hold time	$t_{SOH}$	50	—	—	ns		
SC pulse width	$t_{SP}$	20	—	—	ns		
SC pulse low time	$t_{SPL}$	20	—	—	ns		
SC setup time for $\overline{CE}$	$t_{SCS}$	0	—	—	ns		
$\overline{CDE}$ setup time for $\overline{WE}$	$t_{CDS}$	0	—	—	ns		
$\overline{CDE}$ hold time for $\overline{WE}$	$t_{CDH}$	20	—	—	ns		
$V_{CC}$ setup time for $\overline{RES}$	$t_{VRS}$	1	—	—	$\mu$ s	$\overline{CE} = V_{IH}$	
$\overline{RES}$ to $V_{CC}$ hold time	$t_{VRH}$	1	—	—	$\mu$ s	$\overline{CE} = V_{IH}$	
$\overline{CE}$ setup time for $\overline{RES}$	$t_{CESR}$	1	—	—	$\mu$ s		
RDY/ $\overline{Busy}$ undefined for $V_{CC}$ off	$t_{DFP}$	0	—	—	ns		
$\overline{RES}$ high to device ready	$t_{BSY}$	—	—	0.3	ms		
$\overline{CE}$ pulse high time	$t_{CPH}$	200	—	—	ns		
$\overline{CE}, \overline{WE}$ setup time for $\overline{RES}$	$t_{CWRS}$	0	—	—	ns		
$\overline{RES}$ to $\overline{CE}, \overline{WE}$ hold time	$t_{CWRH}$	0	—	—	ns		

## HN29V102414T-50H

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Notes
SC setup for $\overline{WE}$	$t_{SW}$	50	—	—	ns		
$\overline{CE}$ hold time for $\overline{OE}$	$t_{COH}$	0	—	—	ns		
SA (2) to CA (2) delay time	$t_{SCD}$	—	—	30	$\mu$ s		
RDY/ $\overline{Busy}$ setup for SC	$t_{RS}$	200	—	—	ns		
Time to device busy	$t_{DB}$	—	—	150	ns		
Busy time on read mode	$t_{RBSY}$	—	45	—	$\mu$ s		

Notes: 1.  $t_{DF}$  is a time after which the I/O pins become open.

2.  $t_{WSD}$  (min) is specified as a reference point only for SC, if  $t_{WSD}$  is greater than the specified  $t_{WSD}$  (min) limit, then access time is controlled exclusively by  $t_{SAC}$ .



**Program, Erase and Erase Verify**

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Write cycle time	$t_{CWC}$	120	—	—	ns		
Serial clock cycle time	$t_{SCC}$	50	—	—	ns		
$\overline{CE}$ setup time	$t_{CES}$	0	—	—	ns		
$\overline{CE}$ hold time	$t_{CEH}$	0	—	—	ns		
Write pulse time	$t_{WP}$	60	—	—	ns		
Write pulse high time	$t_{WPH}$	40	—	—	ns		
Address setup time	$t_{AS}$	50	—	—	ns		
Address hold time	$t_{AH}$	10	—	—	ns		
Data setup time	$t_{DS}$	50	—	—	ns		
Data hold time	$t_{DH}$	10	—	—	ns		
$\overline{OE}$ setup time before command write	$t_{OEWS}$	0	—	—	ns		
$\overline{OE}$ setup time before status polling	$t_{OEPS}$	40	—	—	ns		
$\overline{OE}$ setup time before read	$t_{OER}$	100	—	—	ns		
Time to device busy	$t_{DB}$	—	—	150	ns		
Auto erase time	$t_{ASE}$	—	1.0	10.0	ms		
Auto program time Program(1), (3)	$t_{ASP}$	—	1.5	20.0	ms		
Program(2)	$t_{ASP}$	—	1.0	20.0	ms		
Program(4), Data recovery write	$t_{ASP}$	—	2.0	30.0	ms		
$\overline{WE}$ to SC delay time	$t_{WSD}$	50	—	—	$\mu$ s		
$\overline{CE}$ pulse high time	$t_{CPH}$	200	—	—	ns		
SC pulse width	$t_{SP}$	20	—	—	ns		
SC pulse low time	$t_{SPL}$	20	—	—	ns		
Data setup time for SC	$t_{SDS}$	0	—	—	ns		
Data hold time for SC	$t_{SDH}$	30	—	—	ns	$\overline{CDE} = V_{IL}$	
SC setup for $\overline{WE}$	$t_{SW}$	50	—	—	ns		
SC setup for $\overline{CE}$	$t_{SCS}$	0	—	—	ns		
SC hold time for $\overline{WE}$	$t_{SCHW}$	20	—	—	ns		

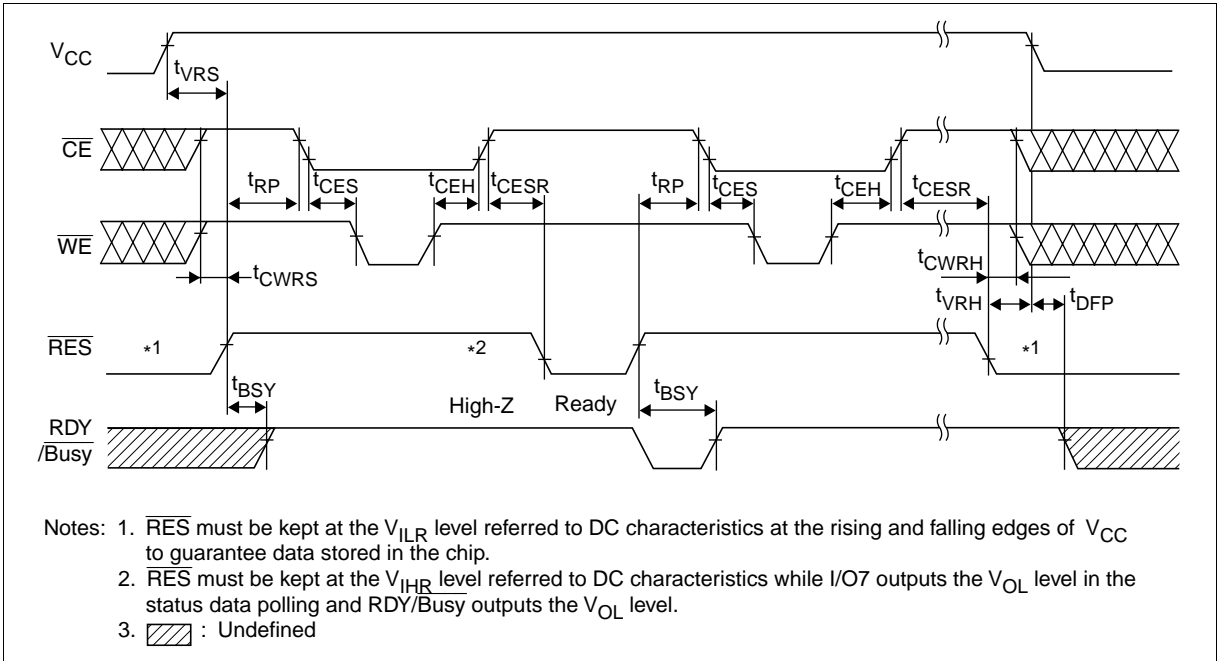
# HN29V102414T-50H

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
$\overline{CE}$ to output delay	$t_{CE}$	—	—	120	ns		
$\overline{OE}$ to output delay	$t_{OE}$	—	—	60	ns		
$\overline{OE}$ high to output float	$t_{DF}$	—	—	40	ns		1
$\overline{RES}$ to $\overline{CE}$ setup time	$t_{RP}$	0.3	—	—	ms		
$\overline{CDE}$ setup time for $\overline{WE}$	$t_{CDS}$	0	—	—	ns		
$\overline{CDE}$ hold time for $\overline{WE}$	$t_{CDH}$	20	—	—	ns		
$\overline{CDE}$ setup time for SC	$t_{CDSS}$	1.5	—	—	$\mu$ s		
$\overline{CDE}$ hold time for SC	$t_{CDSH}$	30	—	—	ns		
Next cycle ready time	$t_{RDY}$	0	—	—	ns		
$\overline{CDE}$ to $\overline{OE}$ hold time	$t_{CDOH}$	50	—	—	ns		
$\overline{CDE}$ to output delay	$t_{CDAC}$	—	—	50	ns		
$\overline{CDE}$ to output invalid	$t_{CDF}$	—	—	100	ns		
$\overline{CE}$ hold time for $\overline{OE}$	$t_{COH}$	0	—	—	ns		
$\overline{OE}$ setup time for SC	$t_{OES}$	0	—	—	ns		
$\overline{OE}$ low to output low-Z	$t_{OEL}$	0	—	40	ns		
SC to output delay	$t_{SAC}$	—	—	50	ns		
SC to output hold	$t_{SH}$	15	—	—	ns		
RDY/Busy setup for SC	$t_{RS}$	200	—	—	ns		
Busy time on read mode	$t_{RBSY}$	—	45	—	$\mu$ s		

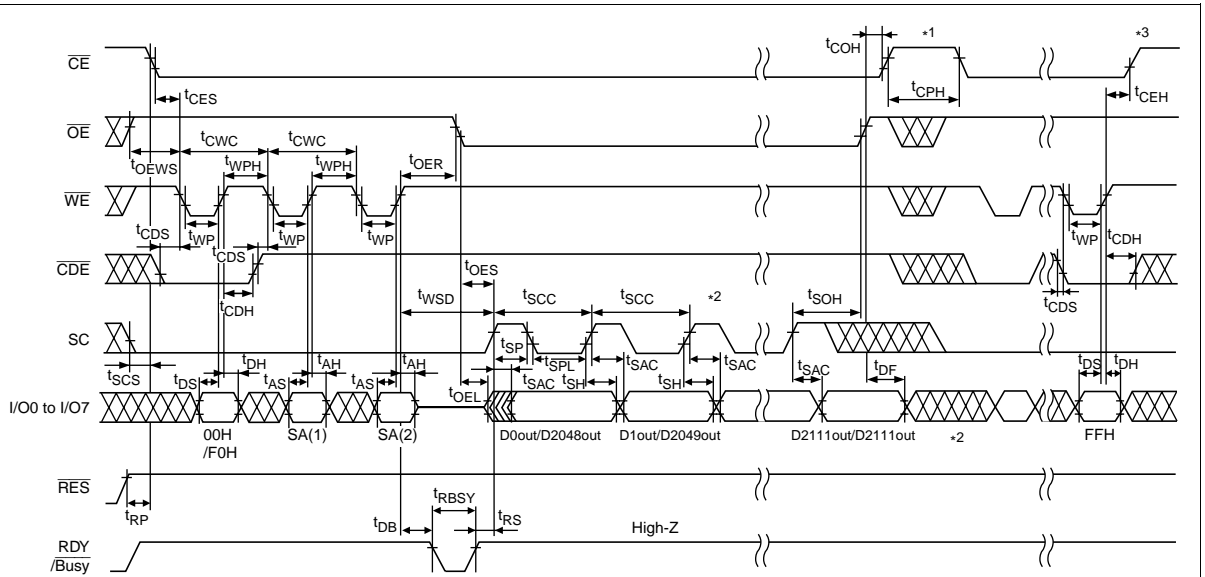
Note: 1.  $t_{DF}$  is a time after which the I/O pins become open.

## Timing Waveforms

### Power on and off Sequence

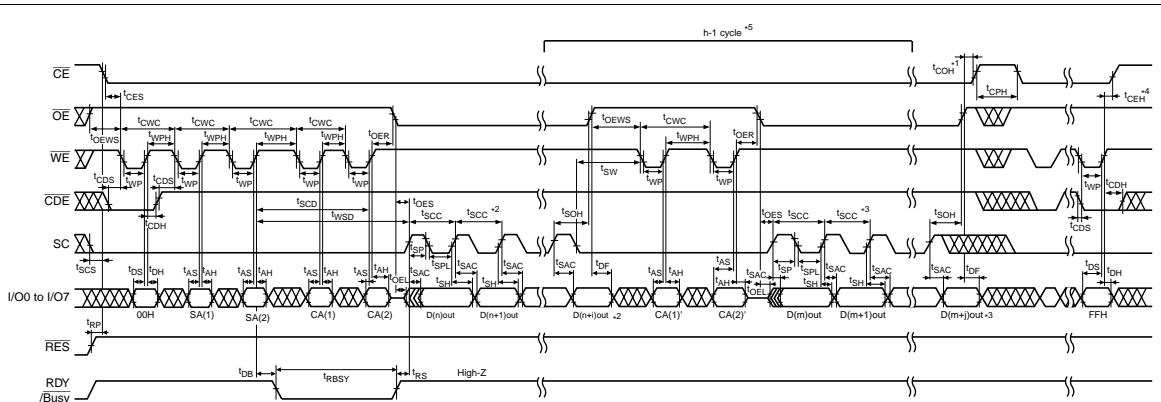


## Serial Read (1) (2) Timing Waveform



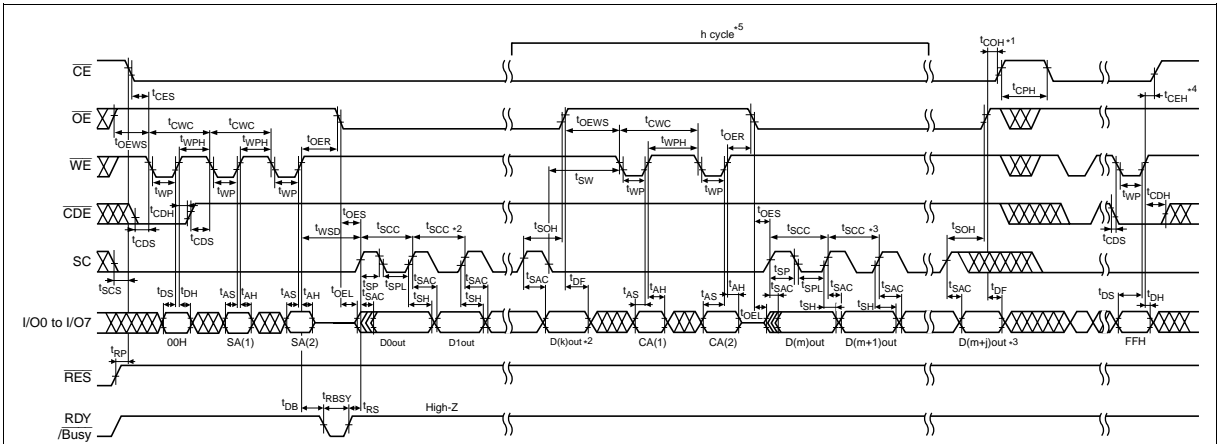
- Notes:
1. The status returns to the standby at the rising edge of  $\overline{CE}$ .
  2. Output data is not valid after the number of the SC pulse exceeds 2112 and 64 in the serial read mode (1) and (2), respectively.
  3. After any commands are written, the status can return to the standby after the command FFH is input and  $\overline{CE}$  turns to the  $V_{IH}$  level.

## Serial Read (1) with CA before SC Timing Waveform



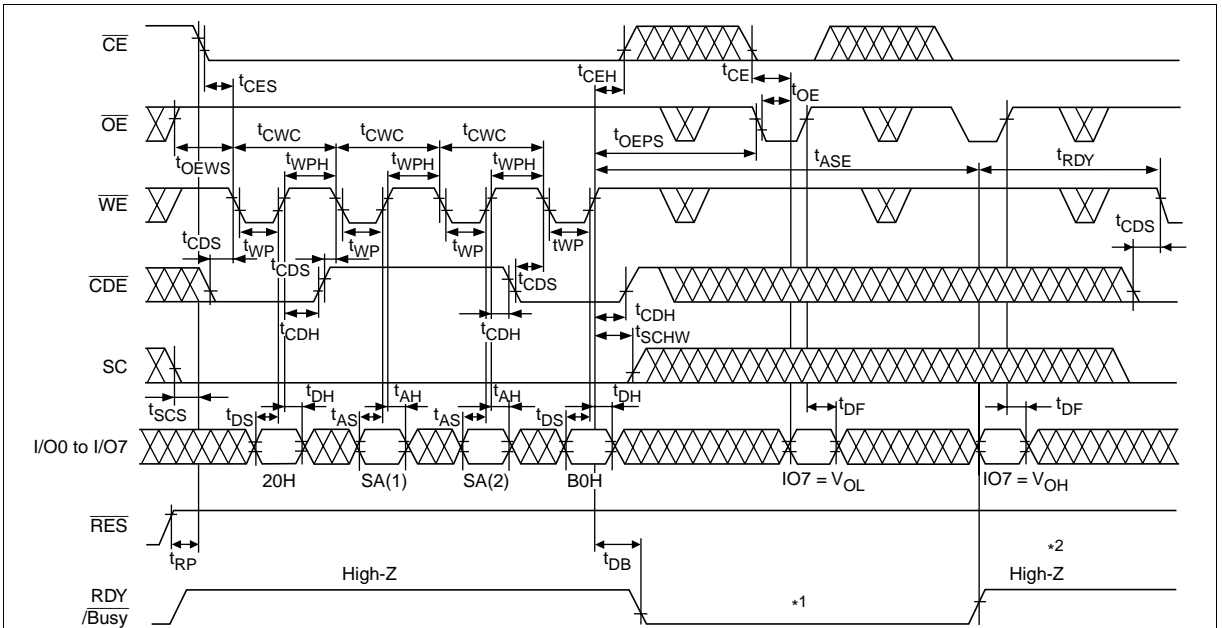
- Notes:
1. The status returns to the Standby at the rising edge of  $\overline{CE}$ .
  2. Output data is not valid after the number of the SC pulse exceeds  $(2112-n)$ . ( $i \leq 2111-n$ ,  $0 \leq n \leq 2111$ )
  3. Output data is not valid after the number of the SC pulse exceeds  $(2112-m)$ . ( $j \leq 2111-m$ ,  $0 \leq m \leq 2111$ )
  4. After any commands are written, the status can return to the standby after the command FFH is input and  $\overline{CE}$  turns to the  $V_{IH}$  level.
  5. This interval can be repeated (h-1) cycle. ( $1 \leq h \leq 2048 + 64$ )

Serial Read (1) with CA after SC Timing Waveform



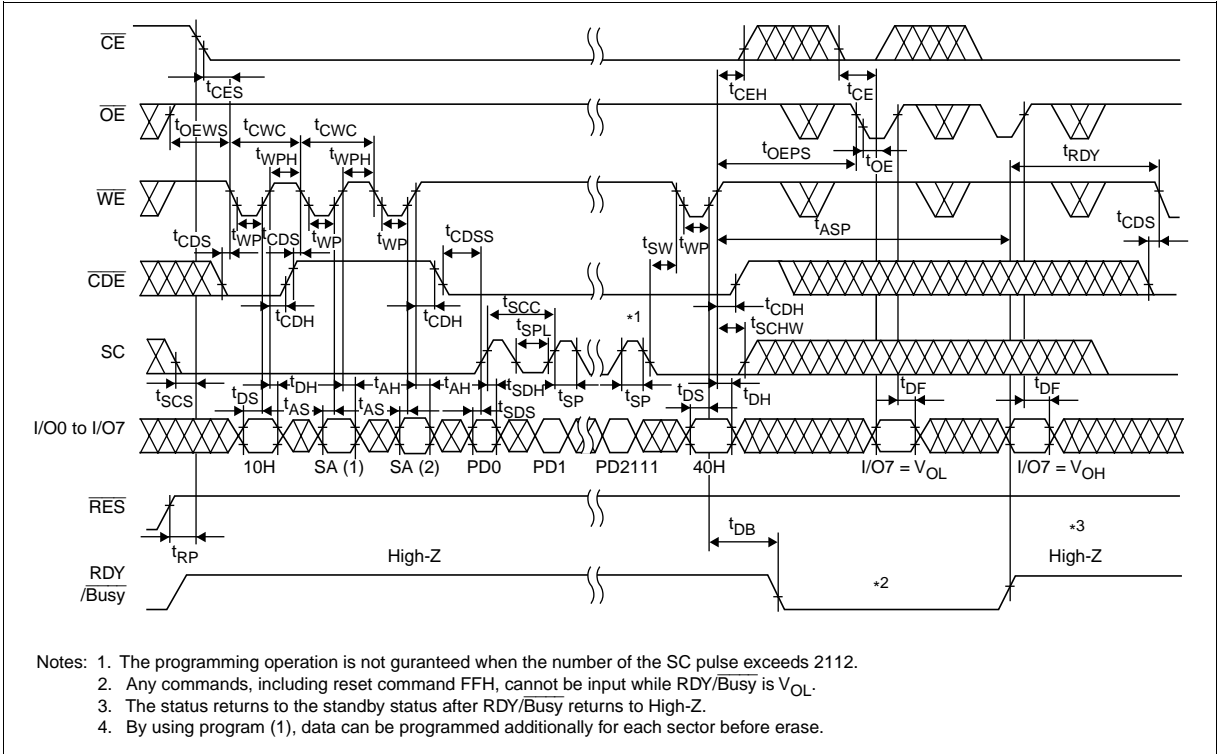
- Notes:
1. The status returns to the Standby at the rising edge of  $\overline{CE}$ .
  2. Output data is not valid after the number of the SC pulse exceeds 2112. ( $0 \leq k \leq 2111$ )
  3. Output data is not valid after the number of the SC pulse exceeds  $(2112-m)$ . ( $j \leq 2111-m, 0 \leq m \leq 2111$ )
  4. After any commands are written, the status can return to the standby after the command FFH is input and  $\overline{CE}$  turns to the  $V_{IH}$  level.
  5. This interval can be repeated h cycle. ( $1 \leq h \leq 2048 + 64$ )

Erase and Status Data Polling Timing Waveform (Sector Erase)

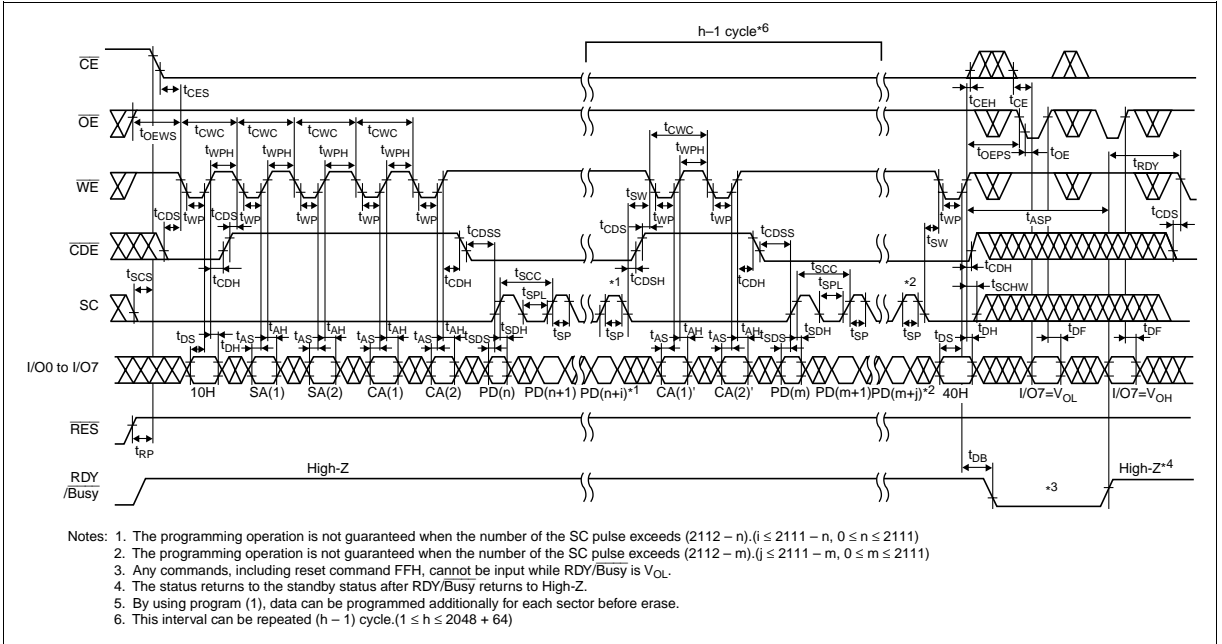


- Notes:
1. Any commands, including reset command FFH, cannot be input while RDY/Busy outputs a  $V_{OL}$ .
  2. The status returns to the standby status after RDY/Busy returns to High-Z.

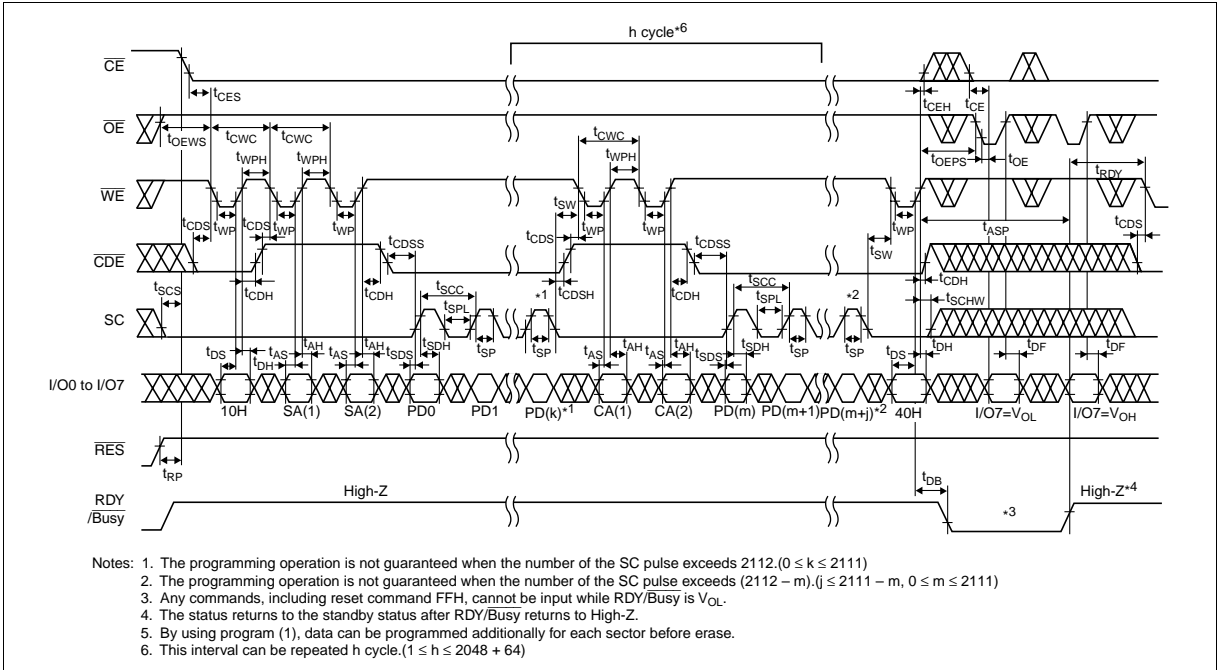
## Program (1) and Status Data Polling Timing Waveform



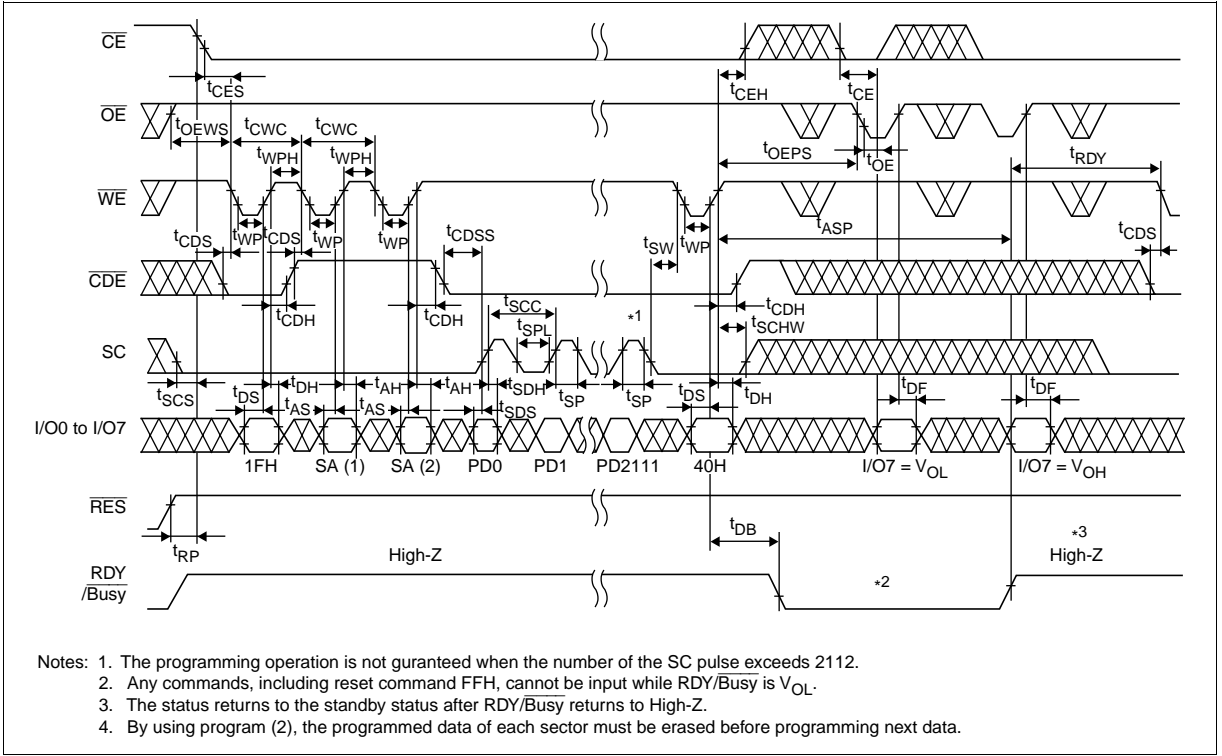
Program (1) with CA before SC and Status Data Polling Timing Waveform



Program (1) with CA after SC and Status Data Polling Timing Waveform

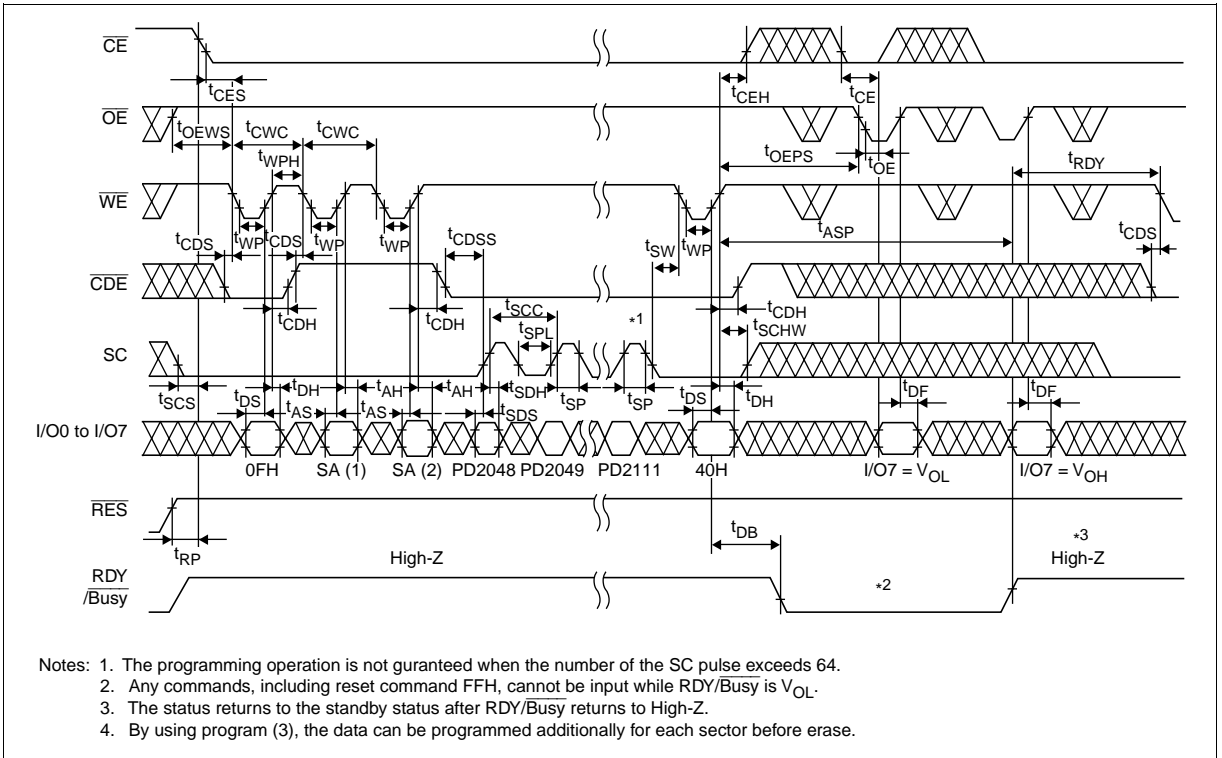


## Program (2) and Status Data Polling Timing Waveform

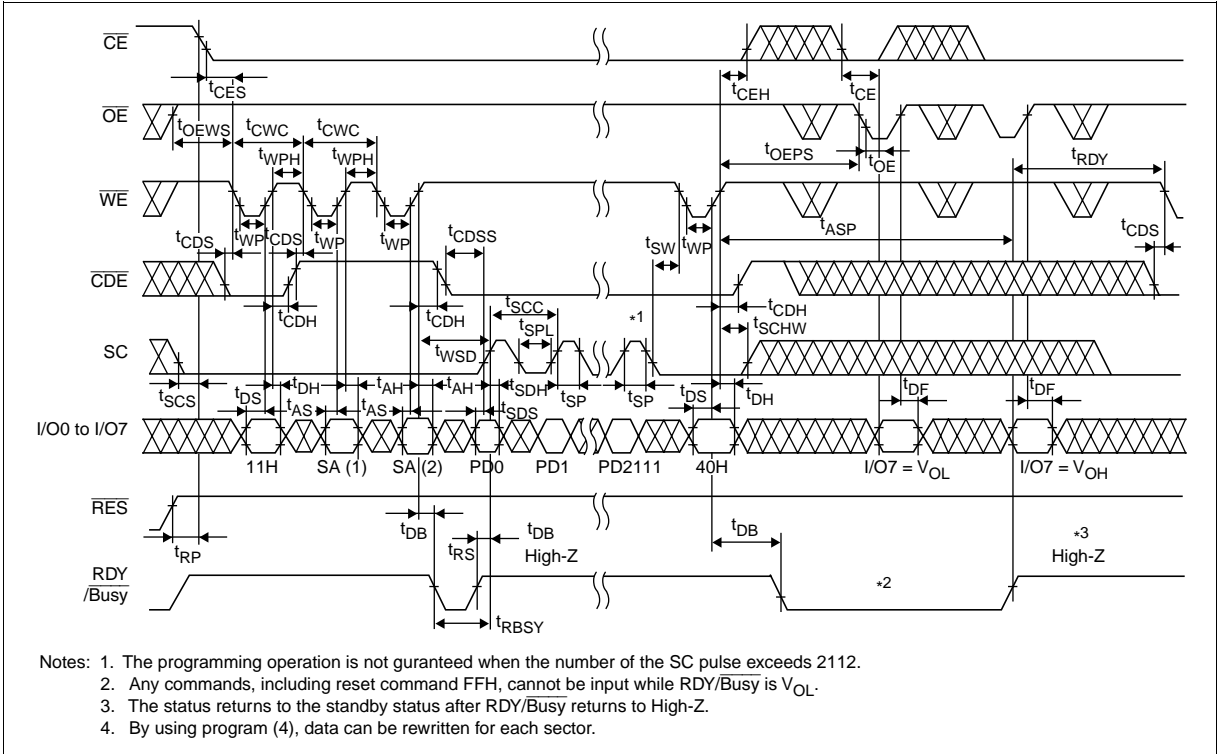




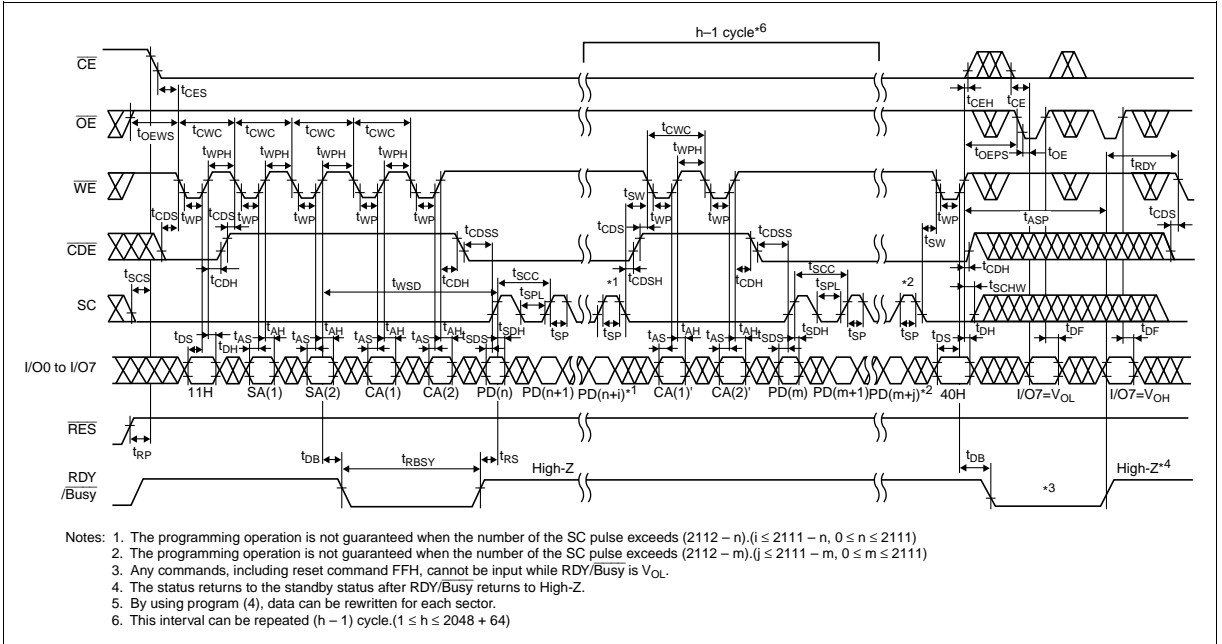
Program (3) and Status Data Polling Timing Waveform



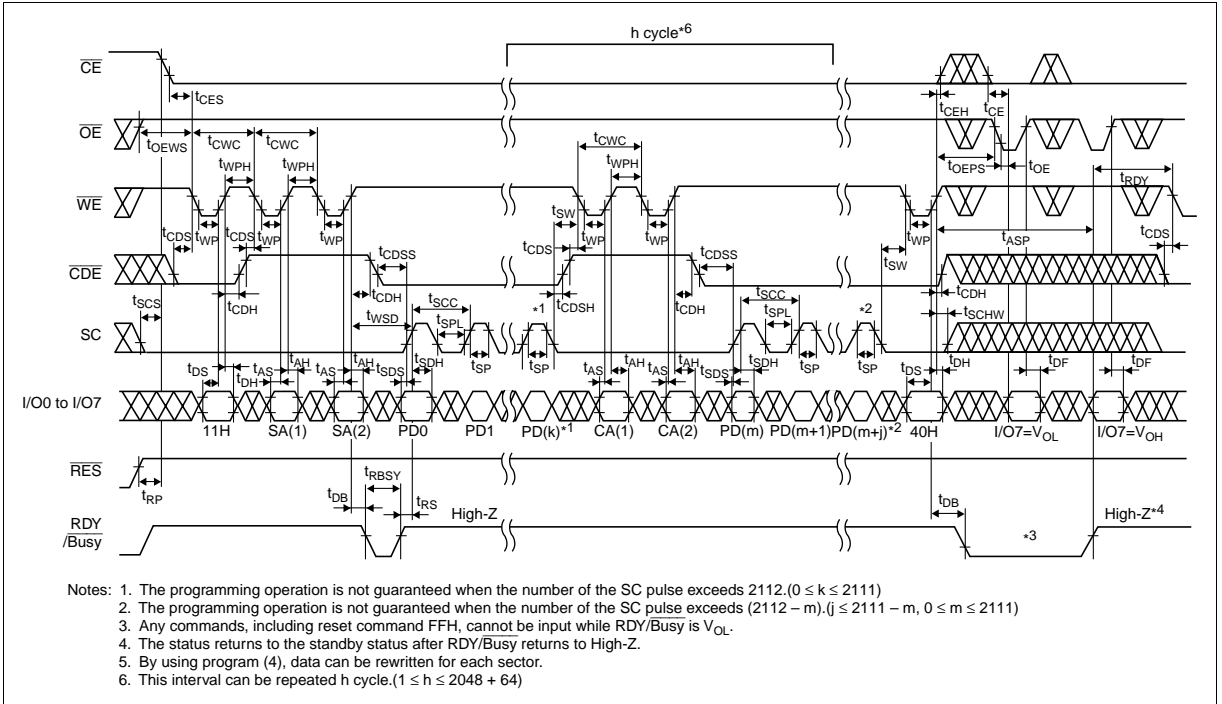
## Program (4) and Status Data Polling Timing Waveform



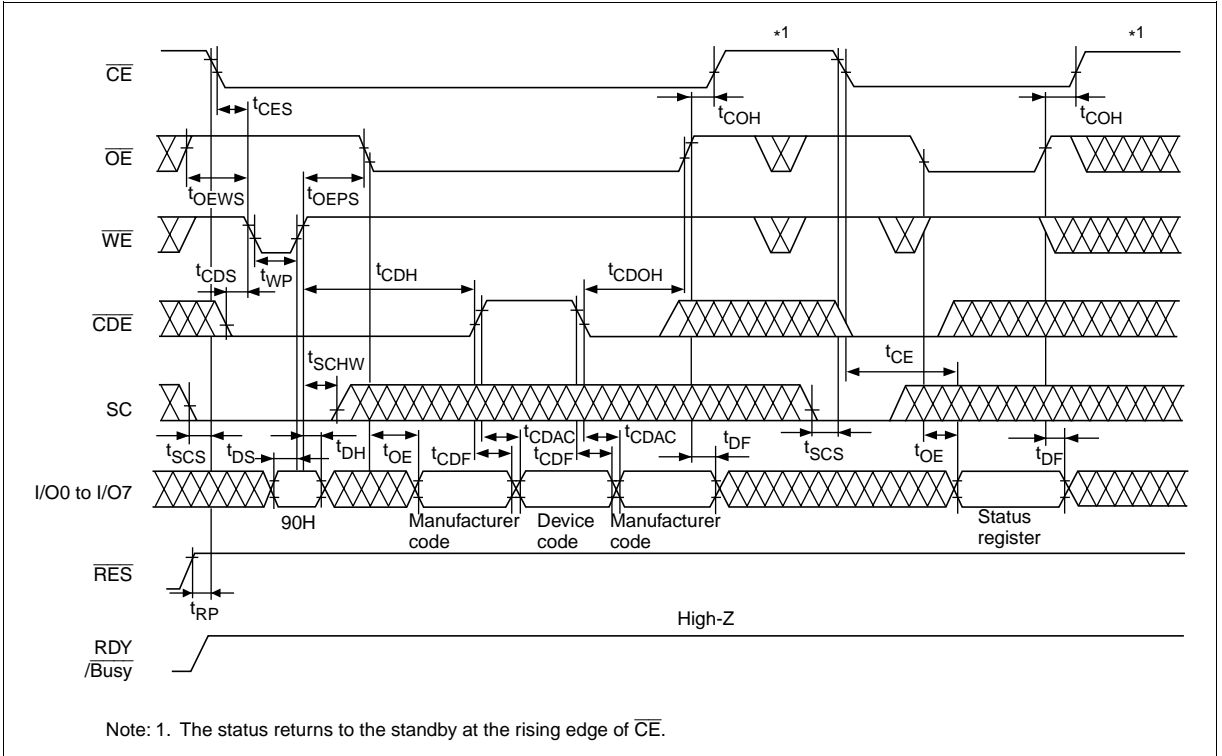
Program (4) with CA before SC and Status Data Polling Timing Waveform



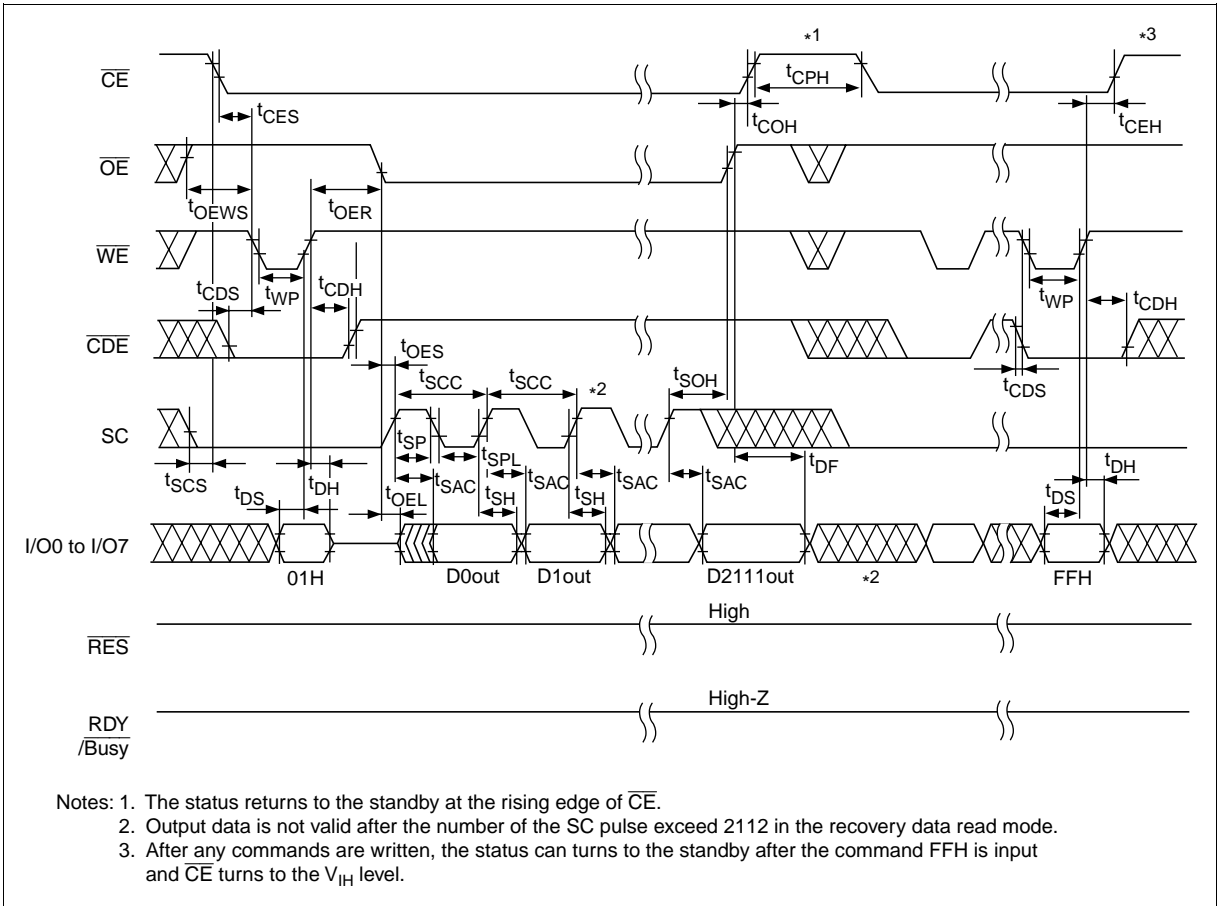
Program (4) with CA after SC and Status Data Polling Timing Waveform



## ID and Status Register Read Timing Waveform

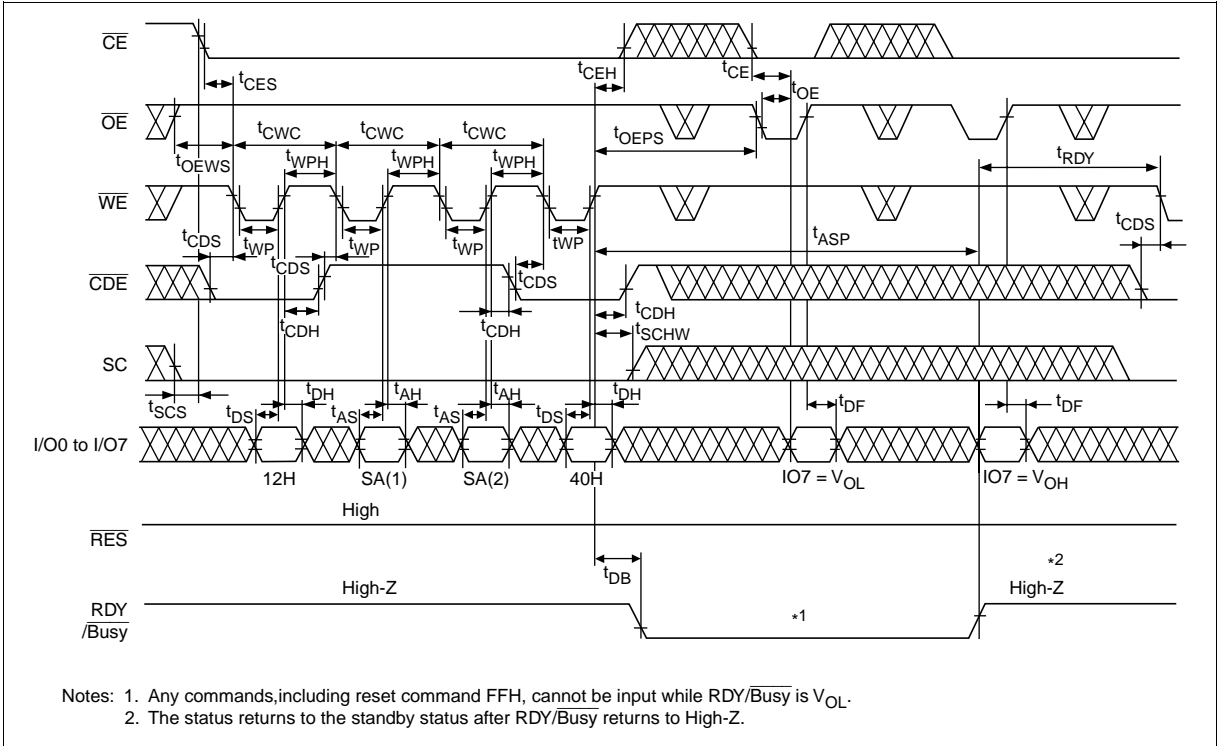


Data Recovery Read Timing Waveform

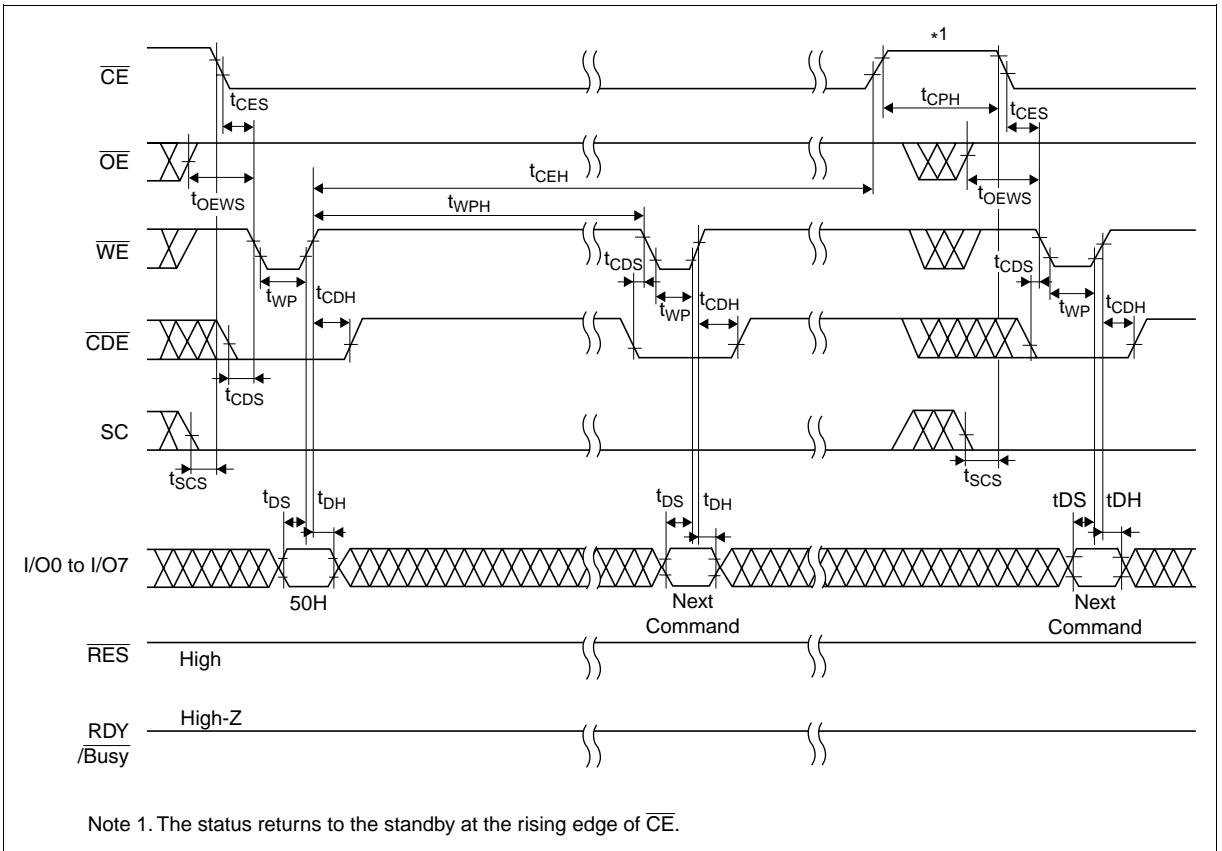


# HN29V102414T-50H

## Data Recovery Write Timing Waveform



Clear Status Register Timing Waveform



## Function Description

**Status Register:** The HN29V102414T-50H outputs the operation status data as follows: I/O7 pin outputs a  $V_{OL}$  to indicate that the memory is in either erase or program operation. The level of I/O7 pin turns to a  $V_{OH}$  when the operation finishes. I/O5 and I/O4 pins output  $V_{OL}$ s to indicate that the erase and program operations complete in a finite time, respectively. If these pins output  $V_{OH}$ s, it indicates that these operations have timed out. If I/O6 pin outputs  $V_{OH}$ , it indicates a possibility that can be corrected by ECC, choose data correction by ECC or not by reading out the data. When these pins monitor, I/O7 pin must turn to a  $V_{OH}$ . To execute other erase and program operation, the status data must be cleared after a time out occurs. From I/O0 to I/O3 pins are reserved for future use. The pins output  $V_{OL}$ s and should be masked out during the status data read mode. The function of the status register is summarized in the following table.

I/O	Flag definition	Definition
I/O7	Ready/Busy	$V_{OH}$ = Ready, $V_{OL}$ = Busy
I/O6	Program/Erase ECC check	When I/O7 outputs $V_{OH}$ , $V_{OH}$ = ECC available, $V_{OL}$ = ECC not available.
I/O5	Erase check	$V_{OH}$ = Fail, $V_{OL}$ = Pass
I/O4	Program check	$V_{OH}$ = Fail, $V_{OL}$ = Pass
I/O3	Reserved	Outputs a $V_{OL}$ and should be masked out during the status data polling mode.
I/O2	Reserved	
I/O1	Reserved	
I/O0	Reserved	

### ECC Applicability

I/O7	I/O6	I/O5	I/O4	System data correction by ECC
$V_{OH}$	$V_{OH}$	$V_{OH}$	$V_{OL}$	Needed
$V_{OH}$	$V_{OL}$	$V_{OH}$	$V_{OL}$	Not needed. Sector replacement
$V_{OH}$	$V_{OH}$	$V_{OL}$	$V_{OH}$	Needed
$V_{OH}$	$V_{OL}$	$V_{OL}$	$V_{OH}$	Not needed. Sector replacement

This device needs to be corrected failure data by ECC on system or Spare sectors, by reading out again the failure sector data when program/erase error occurs.



## Requirement for System

### Specifications

Program/Erase Endurance:  $3 \times 10^5$  cycles

<b>Item</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>
Usable sectors (initially)	64,226	—	65,536	sector
Spare sectors (1-chip operation)	579	—	—	sector
(2-chip operation)	1158	—	—	sector
ECC (Error Correction Code)	3	—	—	bit/sector

## Unusable Sector

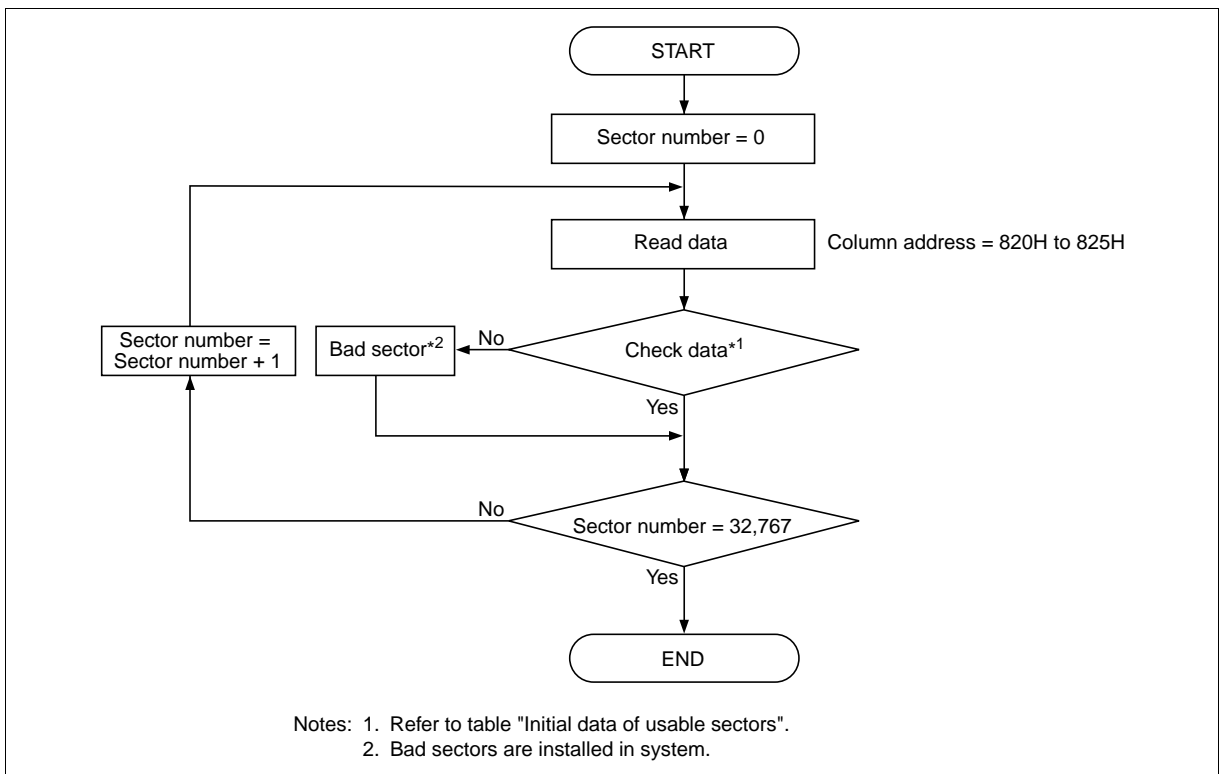
Initially, the HN29V102414T-50H includes unusable sectors. The unusable sectors must be distinguished from the usable sectors by the system as follows.

1. Check the partial invalid sectors in the devices on the system. The usable sectors were programmed the following data. Refer to the flowchart "Indication of unusable sectors".

### Initial Data of Usable Sectors

Column address	0H to 81FH	820H	821H	822H	823H	824H	825H	826H to 83FH
Data	FFH	1CH	71H	C7H	1CH	71H	C7H	FFH

2. Do not erase and program to the partial invalid sectors by the system.

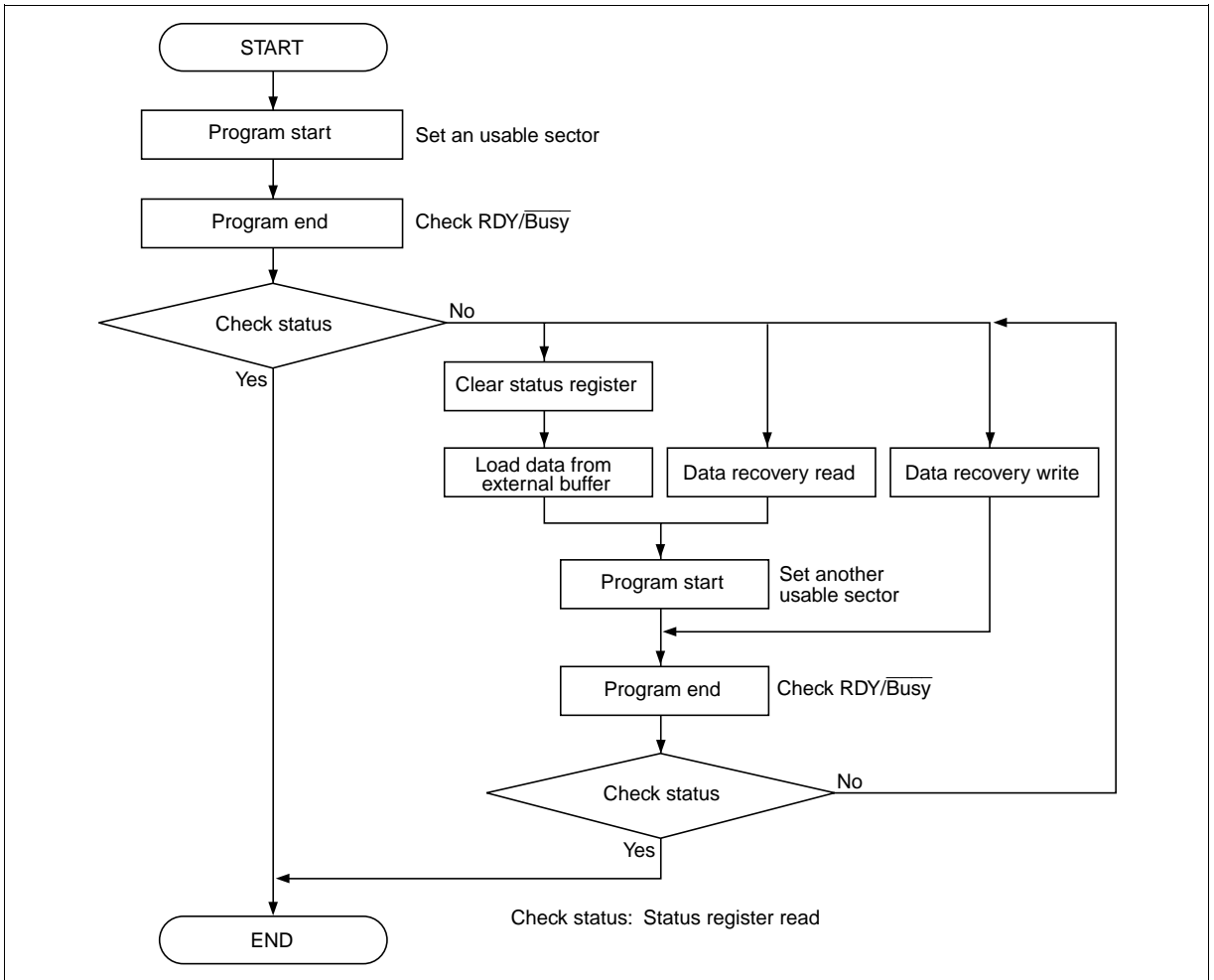


**The Unusable Sector Indication Flow (1-chip)**

### **Requirements for High System Reliability**

The device may fail during a program, erase or read operation due to write or erase cycles. The following architecture will enable high system reliability if a failure occurs.

1. For an error in read operation: An ECC (Error Correction Code) or a similar function which can correct 3-bits per each sectors is required for data reliability. When error occurs, data must not be corrected by replacing to spare sector.
2. For errors in program or erase operations: The device may fail during a program or erase operation due to write or erase cycles. The status register indicates if the erase and program operation complete in a finite time. When an error occurred in the sector, try to reprogram the data into another sector. Avoid further system access to the sector that error happens. Typically, recommended number of a spare sectors are 1.8% (579 sectors/chip (min)) of initial usable 32,113 sectors/chip (min.) by each device. For the reprogramming, do not use the data from the failed sectors, because the data from the failed sectors are not fixed. So the reprogram data must be the data reloaded from the external buffer, or use the Data recovery read mode or the Data recovery write mode (see the “Mode Description” and under figure “Spare Sector Replacement Flow after Program Error”). To avoid consecutive sector failures, choose addresses of spare sectors as far as possible from the failed sectors. In this case,  $10^5$  cycles of program/erase endurance is guaranteed.
3. Prolongation of flash memory life: Due to the life of the memory prolongation, to do wear leveling at about 5000 each. The write/erase endurance is  $3 \times 10^5$  cycles under the condition of the 3-bit error correction and of wear leveling at 5000 each.



**Spare Sector Replacement Flow after Program Error**

**For Errors in program or erase operations**

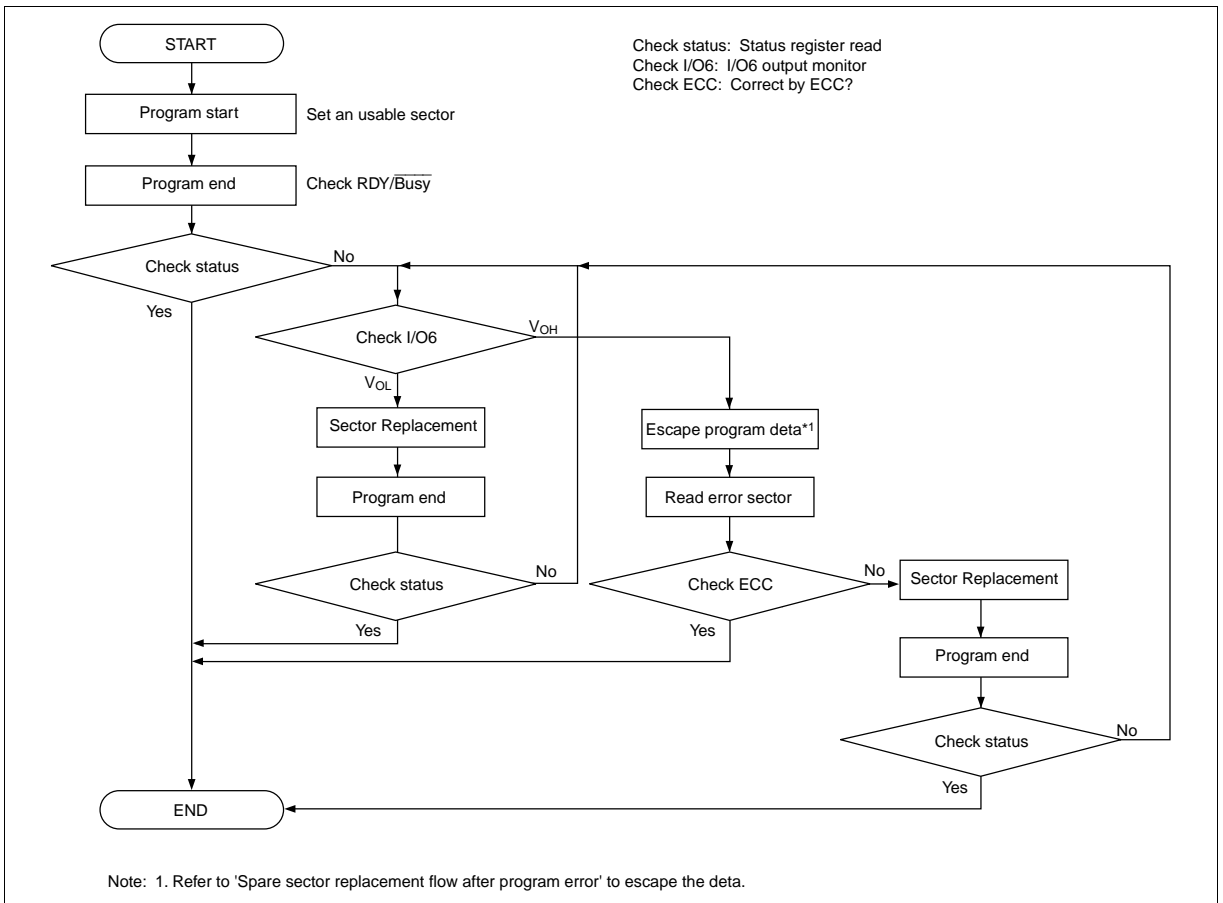
The device may fail during a program or erase operation. Failure mode can be confirmed by read out the status register after complete the erase and program operations. There are two failure modes specified by each codes:

1: Status register error flag:  $I/O6 = V_{OL}$

Replace sector under the “Spare Sectors Replacement Flow at Status Register I/O6 Read”. Replacement must be applied to one sector(2k bytes) which contains failure bits.

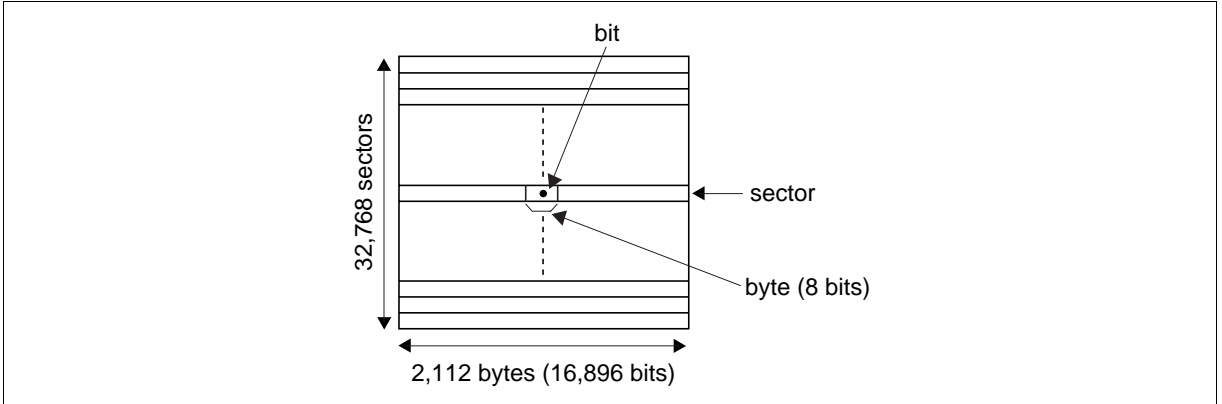
2: Status register error flag:  $I/O6 = V_{OH}$

Escape the program data temporary under the “Replacement Flow at Status Register I/O6 Read”. If failure data can be corrected by ECC, do not replace to spare sector. If failure data can not be corrected by ECC, replace to spare sector. Replacement must be applied to one sector(2k bytes) which contains failure bits.



**Spare Sectors Replacement Flow at Status Register I/O6 Read**

## Memory Structure



Bit: Minimum unit of data.

Byte: Input/output data unit in programming and reading. (1 byte = 8 bits)

Sector: Page unit in erase, programming and reading. (1 sector = 2,112 bytes = 16,896 bits)

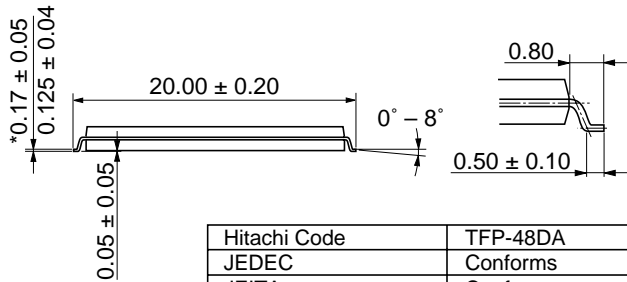
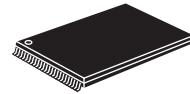
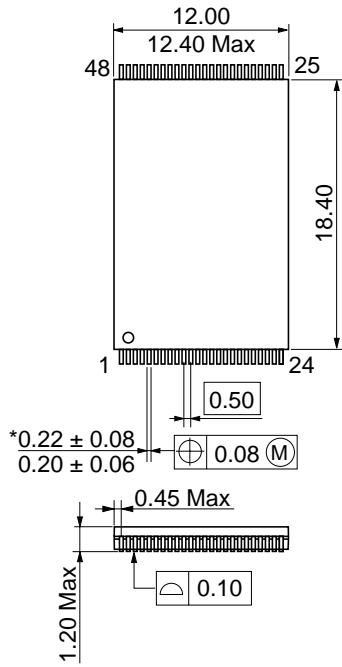
Device: 1 device = 32,768 sectors.

Package Dimensions

HN29V102414T-50H (TFP-48DA)

As of January, 2002

Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	TFP-48DA
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.52 g

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